SERVICE MANUAL

Portable Computer

ZWL-200-2/4

ZENITH | data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, mark the manual and list the information in the record below.

Record of Field Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Chapter 1
Introduction

This manual describes the SupersPort 286 Portable Computer, an 80286 based computer. The SupersPort 286 Portable Computer and the SupersPort Portable Computer, an 8088 based computer, appear almost identical except for the keyboard and LEDs. Be sure that the unit you are working on is the SupersPort 286.

The SupersPort 286 Portable Computer illustrated in Figure 1-1 is a fully PC-compatible computer. It offers full computing capabilities in a small, lightweight package. In performance and power it most closely resembles the Z-286 computer with some obvious differences. The video system uses an advanced LCD controller rather than the more common 6845 controller. It also uses the low-power 80C286 microprocessor and cannot accept expansion cards. Some of its other features are:

- A 25-row, 80-column liquid crystal display with a pixel resolution of 640 x 400. This display uses a double twisted-phneumatic LCD display with an advanced video controller.
- A 79-key keyboard that maintains full PC-compatibility with the standard 84-key keyboard and the 101-key advanced keyboard by using mode switching and multiple keys to duplicate the keypad and special function key operation.
- A keypad interface connector (5-pin DIN). The optional external keypad accessory provides the functionality of the 101-key advanced keyboard.
- RGB video output from a 9-pin connector on the rear panel of the computer.
- One serial communications port (DB-9) and one parallel port (DB-25).
- An external floppy disk drive/tape backup connector (DB-25).
- A real-time clock.
- A rechargeable Nicad battery for portable operation. 4.0 A/Hr rated.
- One internal 1.4M, 3.5-inch floppy disk drive and one internal 20M or 40M, 3.5-inch hard disk drive, depending on the model. An optional external disk drive unit is available with one 360K 5.25-inch drive.
- 1M total memory, expandable to 2M.
- An optional Hayes 1200B- or 2400B-compatible modem for data communication over telephone lines.
- A 120/240 volt AC auto-switching power line adapter.
- An optional 12-volt DC automotive cigarette lighter adapter.

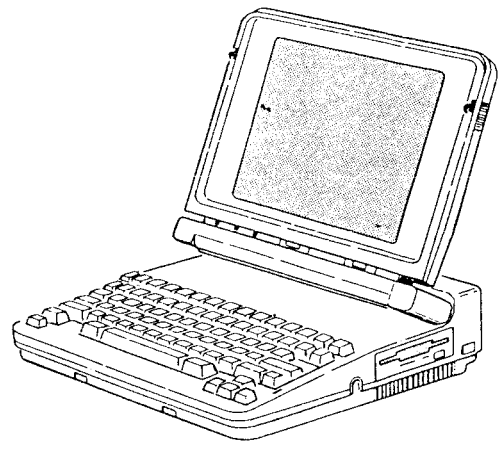

Figure 1-1. SupersPort 286 Portable Computer

Optional Equipment

Table 1-1 lists the hardware options available for the SupersPort 286 computer.

Table 1-1. Hardware Options

HARDWARE OPTION	MODEL NUMBER
12-volt DC cigarette lighter adapter	ZA-181-7
24 key numeric keyboard	ZA-3034-NP
Expansion chassis and connector	ZAS-3034-EV
Extended/EMS expansion memory (1M)	ZA-180-66
Hayes 1200B-compatible modem	ZA-181-19
Hayes 2400-compatible modem	ZA-181-20

Related Publications

SupersPort 286 Portable Computer Owner's Manual **(595-4107)** — This manual, provided with the computer, describes the installation and operation of the computer for the user. It includes a brief description of the hardware, its configuration, and basic maintenance.

You may also find the following publications useful. They are available from Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

Intel IAPX 286 Hardware Reference Manual — This manual provides an in-depth study of the 80286 microprocessor and the 80287 numeric coprocessor.

Intel IAPX 286 Programmer's Reference Manual — This manual Provides information on the architecture of the 80286, including its basic and extended instruction sets. Also includes detailed information about CPU addressing modes, memory management, and system control.

MS-DOS Programmer's Utility Pack **(CB-3163-30)** — This software package from Zenith Data Systems contains information and software to write and assemble MS-DOS and 8088 and 80286 assembly language programs. Separate packages are available for MS-DOS version 2 and MS-DOS version 3.

Specifications

CPU

Processor:	80C286 CMOS 16-bit processor.
Type:	32-bit internal.
Clock speed:	Switch selected: 12 MHz or 6 MHz.
Coprocessor:	Optional 80287 numeric data coprocessor.
Memory:	1M dynamic RAM total standard (eight 256-kilobit x 4 devices). Expandable to 2M.
Display:	LCD device.
Capacity:	80 x 25 characters in text mode. 640 x 400 (double-scanned) pixels in graphics mode. PC-compatible in normal text and graphics mode.
Sound:	Miniature transducer.

Input/output

Serial port:	Asynchronous serial RS-232C port (DB-9 connector). 1 start bit, 7- or 8-bit word length, 1 or 2 stop bits. Selectable baud rates of 110, 150, 300, 600, 1200, 2400, 4800, or 9600 baud. RD, CTS, DSR, CD signals recognized. TD, RTS, DTR control signals generated. Half- or full-duplex operation.

Parallel port:	Centronics-type parallel output port (DB-25 connector).
Video:	RGB (color) video with intensity signals. Output is through a 9-pin connector.
Modem:	RJ-11 modular line and telephone connectors. Optional modems: 300/1200 baud (Hayes 1200B compatible) and 300/1200/2400 (Hayes 1200B compatible at 300 or 1200 baud and Hayes 2400 compatible at 2400 baud).
Floppy disk drive:	3.5-inch double-sided, high-density. 1.4M formatted capacity, 135 tpi, 9 sectors per track. Write-protection recognized. Optional external 5.25-inch double-sided, double-density floppy disk drive. 360K formatted capacity, 48 tpi, 9 sectors per track. Write-protection recognized.
Hard disk drive:	3.5-inch 20M or 40M formatted capacity, depending on model.
Keyboard:	79 keys: 60-key alphanumeric typewiter arrangement with four multifunction keys, four cursor control keys, and ten function keys. Full PC-compatibility maintained. by using mode switching and multiple keys to duplicate keypad and special function key operation. Optional external keypad. Provides functionallity of 101-key advanced keyboard.
Power requirements:	+18 VDC (11.4 VDC minimum) at 3.2 A maximum (57.6 watts).
External power line adapter	
Input voltage:	120/240-volt, auto-switching (90 - 260 VAC).
Input frequency:	50 or 60 Hz (48 - 62 Hz).
Current:	2 A maximum continuous under full load.
Output voltage:	16.5 VDC ±5% at 2 A maximum. ±200 mv maximum ripple.
Battery:	12.5 volt (4.0 AHr) NiCad battery pack (removeable) standard - HDD systems. Thermocontrolled charging with overcharge and short circuit protection low battery indicator. Battery life 3.1 hours (heavy user duty cycle). Computer is operational while battery is recharging. Battery life - minimum 200 charge/discharge cycles. Shelf life up to 5 years. Battery pack weight - 3.0 lbs.
Environment	
Operating:	40° - 95° F (5° - 35° C) at 20% - 80% relative humidity (non-condensing).
Storage:	–40° - 125° F (–40° - 51° C) at 20% - 80% relative humidity (non-condensing).

Dimensions:	12.2" wide x 12.2" deep (front to back) x 3" tall at back (31.0 cm x 31.0 cm x 7.8 cm) with display closed. 11.5" tall (29.2 cm) with display in full upright position.
Weight	10.2 lbs (3.8 kg) with standard configuration (two drives, 640K RAM).

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Chapter 2
Setup

This chapter discusses the installation and setup of the SupersPort 286 Portable computer for service operation.

Preparation

Recommended Environment — Setup the SupersPort 286 computer in an envirnment that meets the specifications listed in Chapter 1 for normal operating conditions. Remove all peripherals and non-Zenith additions to the hardware before you test the computer. This helps determine whether a problem exists in the SupersPort 286 computer itself or in a peripheral device.

Power Requirements — Choose a dependable source of electrical power that is free of surges and transients before you test the computer. If a charged battery is used, make sure the battery has been charged for at least eight hours.

Configuration — The configuration of the SupersPort 296 computer is accomplished through firmware built into the computer. The Setup/-Configuration menu is part of the Monitor program. Refer to Chapter 4 for configuration.

Power Connections

The computer can operate from any one of three different power sources: the battery pack, the external AC power line adapter (either 120 or 240 VAC) or 12 VDC. Each source requires the use of a different adapter.

The AC adapter senses the line voltage and automatically switches to operate at either 120 VAC or 240 VAC. It contains a step-down transformer and DC bridge rectifier to produce the nominal +16.5 VDC. The 12-volt DC adapter contains no circuitry and operates from a automobile cigarette lighter adapter.

The adapters connect to the DC power jack on the rear of the computer or battery pack. Figure 2-1 illustrates the location of the DC power jack and the ON/OFF switch. An adapter can be plugged into the battery pack without interrupting the computers operation. The adapter starts recharging the battery when you plug it into the battery pack.

CAUTION

Do not use the DC adapter to power the computer unless a battery pack is attached to the computer. Do not attempt to start a motor vehicle while the Dc adapter is being used with the computer. The starting circuits of most motors transients back through the power system that could damage the computer or cause it to malfunction.

Figure 2-1 illustrates the correct procedure for connecting an adapter into an operating computer. First, plug the adapter into its power source, than plug it into the computer. the adapter will not interrupt power from the battery when you plug it in. However, if you do not first plug the adapter into the power source, the adapter can load down a partially discharged battery and interrupt the computer's operation.

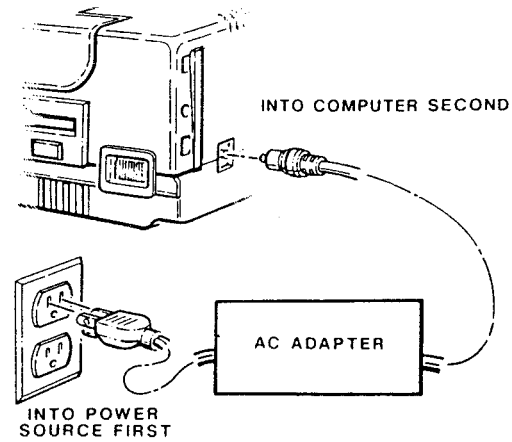


Figure 2-1. Connecting the Adapter

NOTE: If power is applied with the case closed, an audible warning will be heard.

Operation

Refer to Figure 2-2 and slide the latches on each side of the top toward the front of the computer. Lift the display up to a vertical position. Adjust the screen for the most comfortable viewing angle.

NOTE: The latches used on the SupersPort 286 computer will only open with the computer in a horizontal position. This prevents the top from opening during transportation and possibly damaging the computer.

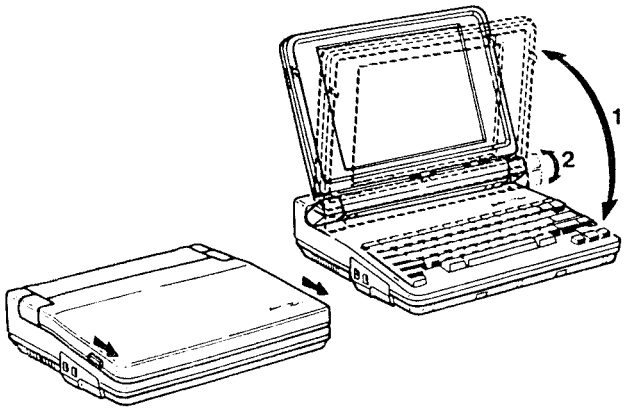


Figure 2-2. Opening the Computer

The floppy disk drive is on the right side of the computer and is drive A. The hard drive is on the left side of the computer and is drive C.

The floppy disk drives used in the SupersPort 286 computer are equipped with an auto-lock feature to protect the read/write heads whenever there is not a disk installed in the drive.

To place a disk in the drive, position the disk with the label facing up and the metal cover toward the drive as shown in Figure 2-3. Insert the disk in the disk load slot and slide the disk all the way into the drive until it latches into place.

To release the disk from the drive, press the eject button.

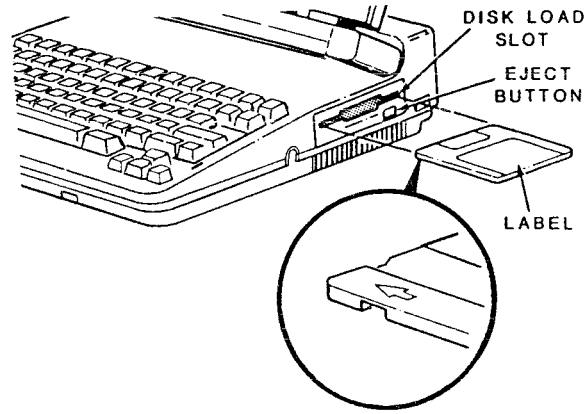


Figure 2-3. Inserting a Disk

Test Bench Power-Up

At this time you are ready to apply power to the computer. Check the following points to make sure the system is ready to have power applied.

- An AC adapter is properly connected.
- The computer display is in an upright position.
- A bootable system disk is installed in drive A.
- All peripherals are disconnected. After testing the computer, you can reattach the peripherals to check their operation.

After checking these items, apply power by sliding the ON/OFF switch to the ON position (toward the front of the computer).

The power-up sequence for the SupersPort 286 computer is similar to other Zenith computers with a few exceptions. The following paragraphs describe the sequence as it occurs during normal system operation.

When you apply power to the computer, the backlight of the LCD display will come on. The display clears both the top and bottom halves at the same time, then after about a two second delay, a cursor will begin flashing in the upper-left corner of the display.

Next, the computer performs a number of internal power-up tests similar to other Zenith computer products. The SupersPort computer does not have

internal LEDs to report the status of these tests, but the tests include the same tests in the same sequence used in other Zenith computers. If the computer completes these tests successfully, it attempts to boot the disk installed in drive A.

After approximately five seconds, the screen will blink and the disk access LED for drive A will light. On initial power-up, the system will attempt to boot drive A. If there is no disk in drive A, the computer will attempt to boot to the default partition of the hard disk. You can defeat autoboot or change the autoboot procedure on the SupersPort computer by changing an entry in the Setup/Configuration menu, refer to Chapter 4 for information on the Setup/-Configuration menu. You can also abort or bypass the autoboot sequence by pressing the ESC key after the boot sequence has started. When you bypass the autoboot sequence, the Monitor prompt (->) will appear on the screen.

If a disk is not installed in drive A, the computer will attempt to load the operating system from the default partition of the hard drive. If the default partition does not contain an operating system, an error message will appear. You can then reset the computer to the Monitor program by pressing the ESC key. If the default partition contains an operating system, the system will complete the boot-up operation.

If the computer completes all operations normally, the computer will load the operating system. You can now load disk-based test software to continue testing the system. You can reset the computer at any time by pressing CTRL-ALT-DEL. This restarts the power-up and autoboot sequence. You can reset the computer to the Monitor program by pressing CTRL-ALT-INS.

After testing the computer, use the following steps to power down the computer. This sequence prevents accidental damage that could extend your service time and costs.

1. Remove all disks.

2. Turn off the power to conserve battery power and prevent unintended operation of the computer.

3. Close and latch the computer to stabilize the cabinet.

80287 Coprocessor Installation

The SupersPort computer supports an 80287 coprocessor. To install a numeric coprocessor:

1. Turn the computer off. If the external AC power supply is attached to the computer, disconnect it.

2. Close and latch the lid.

3. Place a soft cloth on your work surface and turn the computer upside down on your work surface.

4. Carefully pry up on the coprocessor cover, as shown in Figure 2-4.

CAUTION

ICs are complex electronic devices that can be damaged by static electricity. Once you remove the IC from its protective foam packing, do not lay the IC down or let go of it until it is installed in its socket.

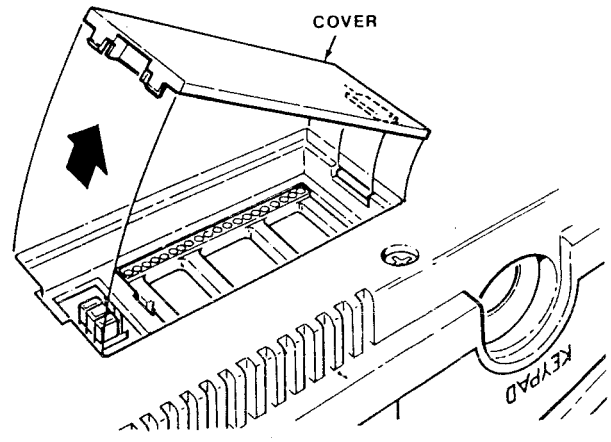


Figure 2-4. Removing the Coprocessor Cover

5. Carefully install the 80287 coprocessor IC. Press the IC firmly into the socket.

NOTE: A pin can become bent under the IC and will appear to be correctly seated in its socket. If a malfunction occurs while testing, examine the IC (and remove it, if necessary) to be certain that all pins are correctly inserted.

6. Replace the coprocessor cover.

Chapter 3

Disassembly

Removing the Battery Pack

Refer to Figure 3-1 for the following steps.

1. Turn off the computer and disconnect all peripherals.
2. Press the battery pack button and swing the button end of the battery pack away from the computer.
3. Pull the battery pack so the catches, labeled A, are free from the computer. Set the battery pack aside.

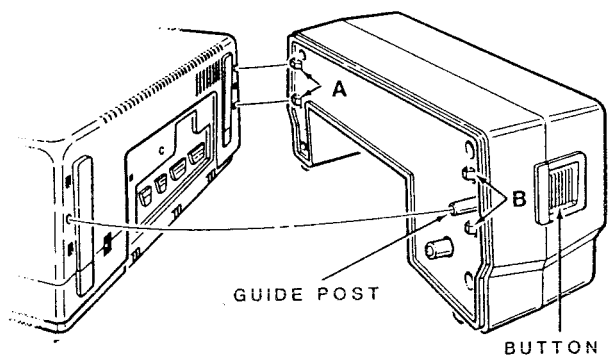


Figure 3-1. Removing the Battery Pack

Removing the Battery

Refer to Figures 3-2 and 3-3 for the following steps.

1. Remove the battery pack, as explained in the "Removing the Battery Pack" section.
2. Open the battery pack by removing the four screws, as shown in Figure 3-2.
3. Disconnect the battery connector from the battery pack 3-pin connector with the connector lock pressed, as shown in the inset of Figure 3-3. Lift the battery from the battery pack and set the battery aside.

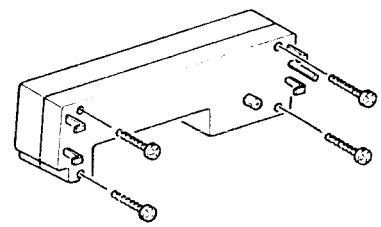


Figure 3-2. Opening the Battery Pack

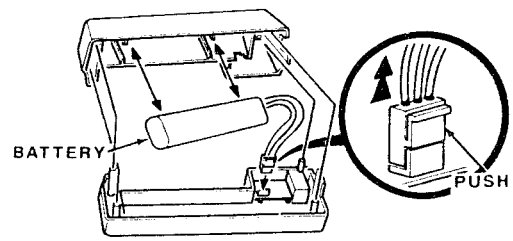


Figure 3-3. Disconnecting the Battery

Separating the Display from the Base Unit

Refer to Figure 3-4 and 3-5 for the following steps.

1. Disconnect the power cord and all peripherals.

2. Place the computer upside down on a clean, soft surface. Remove the seven screws, shown in Figure 3-4, and set the screws aside.

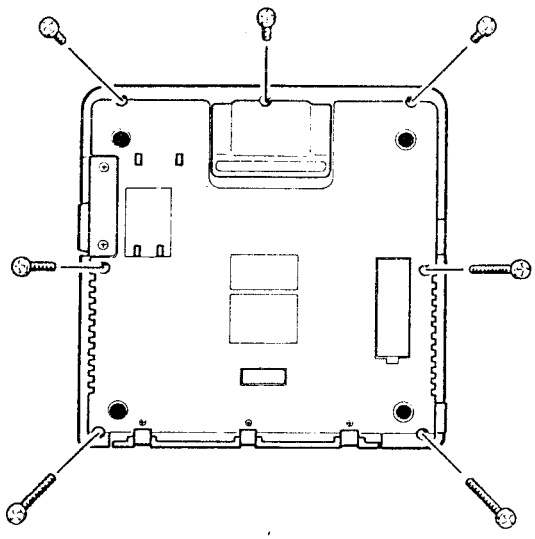


Figure 3-4. Bottom Screws

3. Carefully lift the computer from the keyboard top cover and set it down next to the top cover, as shown in Figure 3-5.

4. Place masking tape on corresponding ends of the display cable and the base unit connector. This is to help you identify the matching ends of the connectors during reassembly. These connectors can be put together wrong (with the ends of the connectors interchanged).

5. Carefully disconnect the display cable from the base unit.

During reassembly, make sure the connectors are joined correctly (the corresponding ends which were marked with masking tape must be joined). Also, make sure the plastic hard drive cover is in place when the top and bottom covers of the base unit are joined.

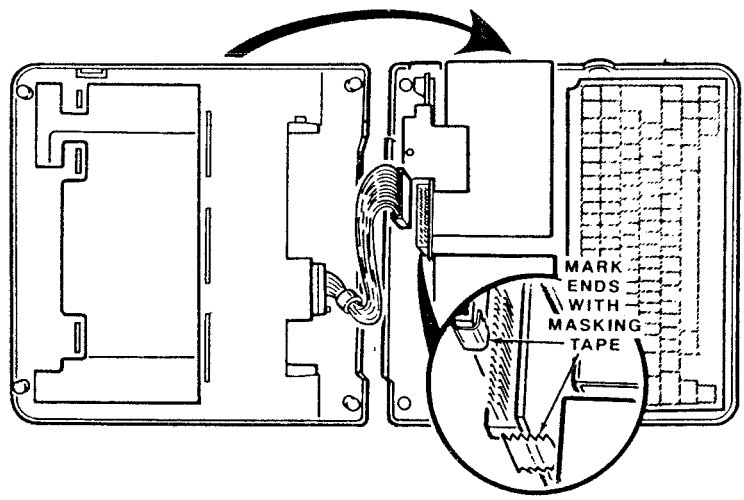


Figure 3-5. Disconnecting the Display

Removing the Keyboard

Refer to Figures 3-6 and 3-7 for the following steps.

1. Separate the display from the base unit as explained in the "Separating the Display from the Base Unit" section.

2. Remove the two screws securing the keyboard to the bottom cover, shown in Figure 3-6. Set the screws aside.

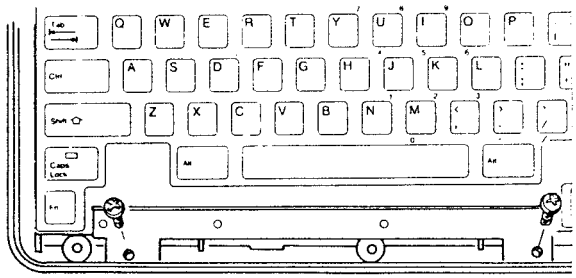


Figure 3-6. Keyboard Screws

3. Remove the ground screw located near the left rear corner of the hard disk drive.

4. Lift the keyboard and lay it face down on the drives, as shown in Figure 3-7.

5. Use a small flat-blade screwdriver to lift the lock of the main board connector CN13 and pull the keyboard ribbon cable from the connector, as shown in the inset of Figure 3-7.

6. Disconnect the keyboard 2-wire cable connector from the main board connector CN19. Set the keyboard aside.

During reassembly, make sure that the keyboard ribbon cable is fully inserted into the connector before you push the connector lock down.

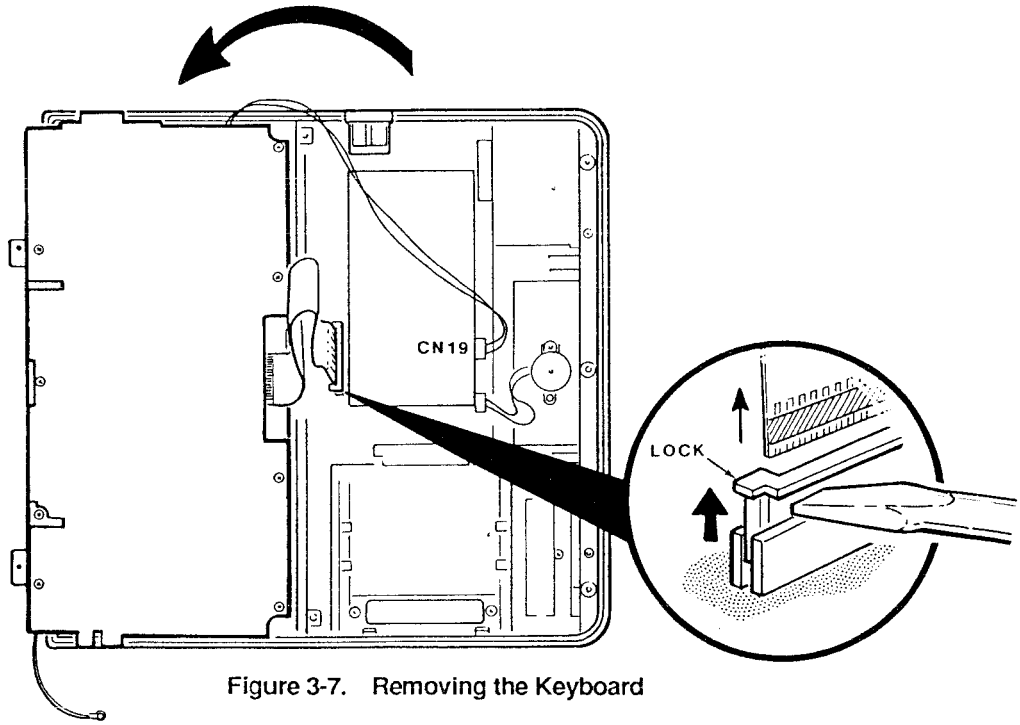


Figure 3-7. Removing the Keyboard

Removing Floppy Drive A

Refer to Figures 3-8 and 3-9 for the following steps.

Observe the position of the drive cables before disassembly so you can return the wires to their original positions during reassembly.

1. Remove the keyboard from the bottom cover, as explained in the "Removing the Keyboard" section.

2. Remove the three screws from the drive A mounting holes, as shown in Figure 3-8. Set the screws aside.

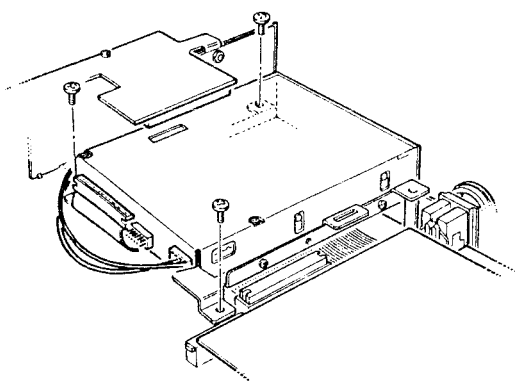


Figure 3-8. Floppy Drive A Screws

3. Lift drive A and move it away from the hard disk drive so you have access to the drive A connectors.

4. Use a small flat-blade screwdriver to disconnect drive A control cable.

5. Use a small flat-blade screwdriver to remove the power connector, as shown in Figure 3-11. Set drive A aside.

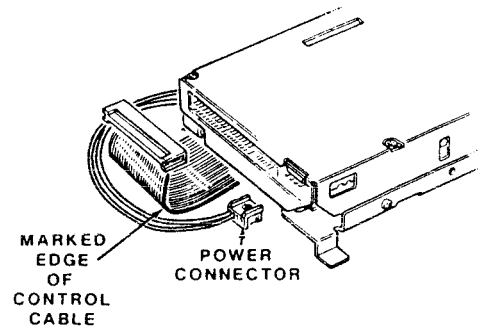


Figure 3-9. Disconnecting Floppy Drive A Power Cable

During reassembly be sure:

- All wires are returned to their original positions.
- To push the power connector all the way on so that it fully engages the drive connector (the cable connector locking tab must be in its matching receptacle).
- The marked wire of the control cable connector must be located as shown in Figure 3-9, and the connectors must be fully engaged.

Removing Hard Drive B and Controller Card

NOTE: The hard drive and controller card are a matched set and must be replaced as a set.

Refer to Figure 3-10 for the following steps.

Observe the position of the drive cables before disassembly so you can return the wires to their original positions during reassembly.

1. Remove the keyboard from the bottom cover, as explained in the "Removing the Keyboard" section.

2. Remove the floppy drive A, as explained in the "Removing Floppy Drive A" section.

3. Remove the three screws from the hard drive B mounting holes, as shown in Figure 3-10. Set the screws aside.

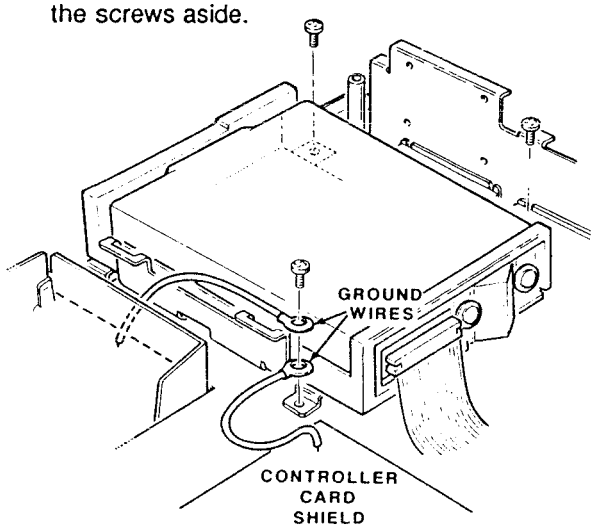


Figure 3-10. Hard Drive B Screws

During reassembly, make sure the ground wire lugs are engaged by the drive mounting screw that is adjacent to the controller card.

Refer to Figure 3-11 for the following steps.

4. Observe the position of the film, ribbon cables, screw, spacer, controller card, and card shield, as shown in Figure 3-11. These items will have to be returned to these positions during reassembly.

5. Disconnect the controller card cable connector from power supply connector CN305.

6. Remove the screw and spacer that secures the controller card and shield. Set the screw, spacer, and shield aside.

7. Disconnect the controller card from main board connector CN15 and set the hard drive and controller card aside.

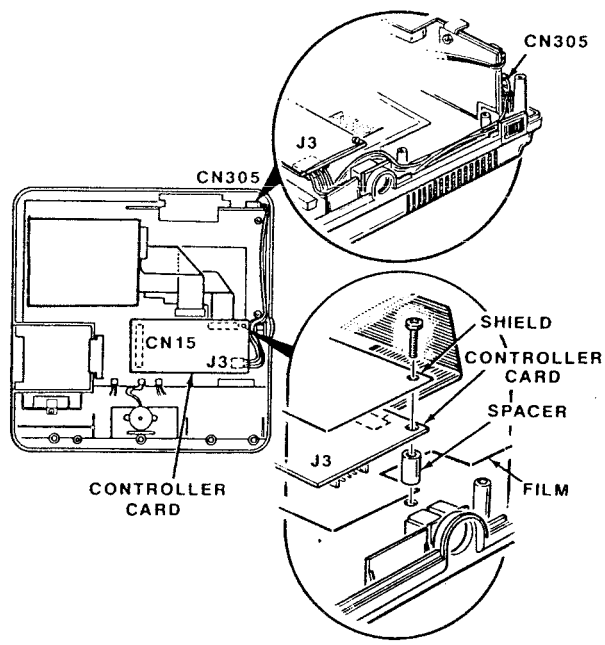


Figure 3-11. Controller Card and Cables

Removing the Power Supply

Refer to Figures 3-12 and 3-13 for the following steps.

1. Separate the display from the base unit, as explained in the "Separating the Display from the Base Unit" section.

2. Disconnect the drive A power cable connector from the power supply connector CN306.

3. Disconnect the controller cable connector from power supply connector CN305.

4. Remove the two screws securing the power supply to the backplate of the computer, as shown in Figure 3-12. Set the screws aside.

5. Remove the screw securing the switch/power jack assembly, as shown in Figure 3-12. Set the screw aside.

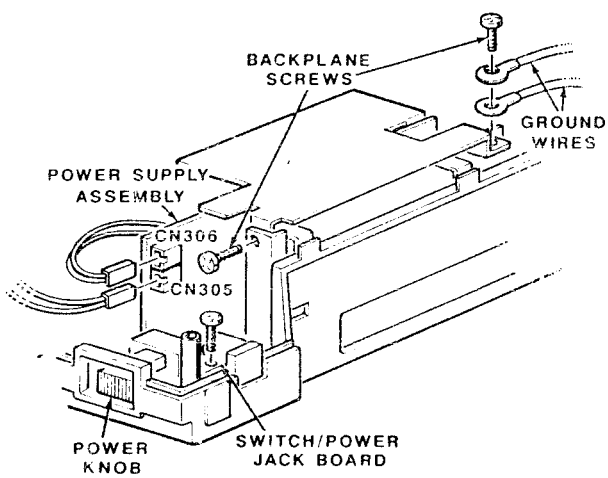


Figure 3-12. Power Supply Screws

6. Lift the power supply from the computer, as shown in Figure 3-13.

7. Remove the switch/power jack board. The fuse on the power supply is now accessible.

During reassembly, make sure:

- The CN401 connector on the switch/power jack board is fully mated to CN301 on the power supply assembly.
- The power switch engages the power knob.
- The connectors on the power supply fully engage the connectors CN6 and CN7 on the main board.

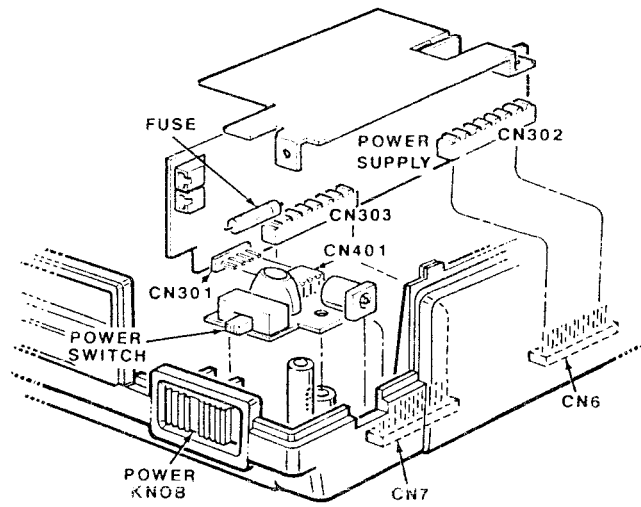


Figure 3-13. Accessing the Fuse

Removing the Main Board

Refer to Figure 3-14 for the following steps.

1. Separate the display from the base unit, a explained in "Separating the Display from the Base Unit" section.

2. Remove the keyboard from the bottom cover, as explained in the "Removing the Keyboard" section.

3. Remove floppy drive A, as explained in the "Removing Floppy Drive A" section.

4. Remove hard drive B and the controller card, as explained in the "Removing Floppy Drive B and Controller Card" section.

5. Remove the power supply, as explained in the "Removing the Power Supply" section.

6. Remove the screw securing main board connector CN11 to the bottom cover, as shown in Figure 3-14. Set the screw aside.

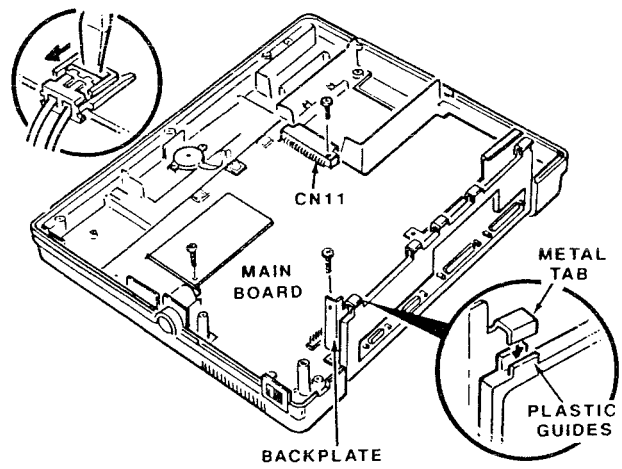


Figure 3-14. Removing the Main Board

8. Remove the screw that secures the computer metal backplate to the bottom cover, as shown in Figure 3-14. Set the screw aside.

9. Use a small flat-blade screwdriver to disconnect the speaker connector, CN14 and lift the main board from the computer.

10. Use a small flat-blade screwdriver to disconnect the battery cable connector from the main circuit board.

During reassembly, make sure the tabs on the metal computer backplate fit into the slots of the plastic back, as shown in the inset of Figure 3-14.

Opening the Display

Refer to Figures 3-15 and 3-16 for the following steps.

1. Turn off power and disconnect all peripherals.

2. Open the computer and lay the display flat facing up, as shown in Figure 3-15. The computer must have its top facing up, as shown in Figure 3-15 in order for the latches to operate, allowing the computer to be opened. The latches will not operate in any other position, keeping the computer from opening accidentally.

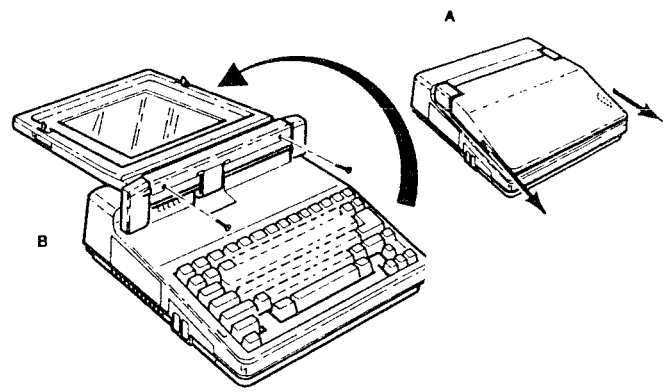


Figure 3-15. Opening the Display

3. Remove the two screws to release the display from the top, as shown in Figure 3-15.

4. Separate the display from the top cover. Locate the wire coming from the shield to the controls assembly, as shown in Figure 3-16.

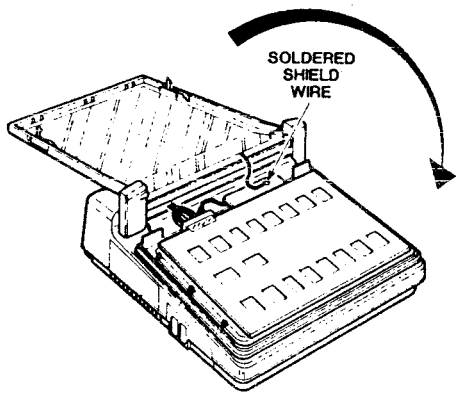


Figure 3-16. Unsoldering the Shield Wire

5. If necessary, unsolder the shield wire from the controls assembly and lay the display face down, on top of the keyboard. Observe the position of all cables connected to the controls assembly, LED assembly, and LCD assembly so that the cables can be positioned in their original locations during reassembly.

Removing the Control Assembly

Refer to Figures 3-17 and 3-18 for the following steps.

1. Open the Display, as explained in the "Opening the Display" section.

2. Remove the two screws securing the contrast and brightness control assembly to the display, as shown in Figure 3-17.

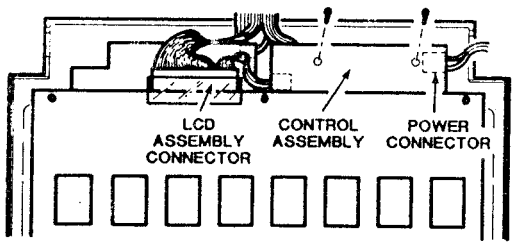


Figure 3-17. Control Assembly Screws

3. Lift the controls assembly and pry cable connectors CN601, CN602, and CN603 from the assembly with a small flat-blade screwdriver, as shown in Figure 3-18. Set the controls assembly aside.

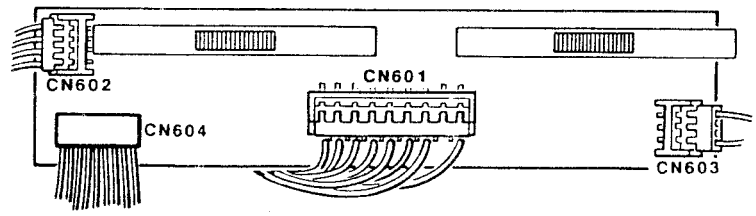


Figure 3-18. Connectors CN601, CN602, and CN603

Removing the LCD Assembly

Refer to Figures 3-19 and 3-20 for the following steps.

1. Open the display according to the "Opening the Display" section.

2. Remove and save the tape covering the LCD board connector solder terminals.

3. Disconnect the cable connector from the LCD assembly connector (see Figure 3-19).

4. Disconnect the power cable connector from the contrast and brightness assembly, as shown in Figure 3-19.

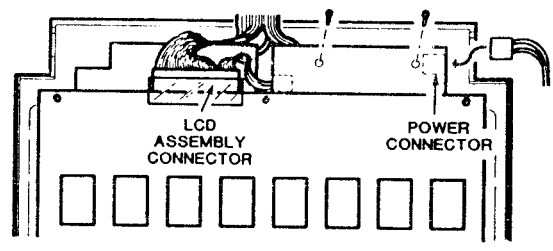


Figure 3-19. Display Board Connectors

5. Remove the three screws A securing the LCD assembly to the display front cover, and loosen three screws B, as shown in Figure 3-20.

6. Lift the LCD assembly from the bottom cover and set aside.

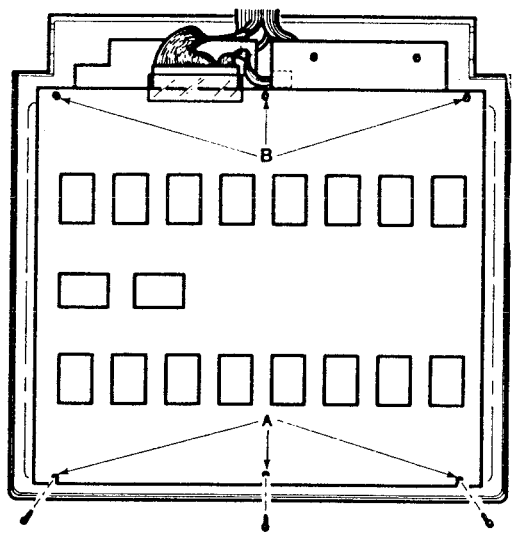


Figure 3-20. LCD Assembly Screws

During reassembly, make sure the tape covers the LCD board connector solder terminals so the do not contact the shield in the top cover.

Removing the LED Assembly

Refer to Figures 3-21 and 3-22 for the following steps.

1. Open the display assembly according to the "Opening the Display" section.

2. Remove the two screws securing the control assembly, turn the assembly over, and disconnect the LCD cable connector from control assembly connector CN604.

3. Disconnect the LCD assembly connector, as shown in Figure 3-21.

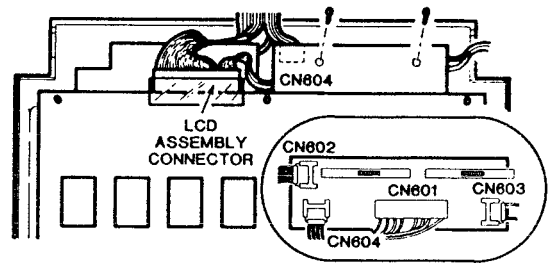


Figure 3-21. LCD Assembly Connector

4. Remove the screw securing the LED assembly to the front cover, as shown in Figure 3-22.

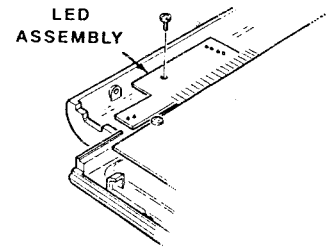


Figure 3-22. LED Assembly Screw

5. Refer to Figure 3-20 to loosen screws B and remove screws A from the LCD assembly. Move the LCD assembly so it does not interfere with the LED assembly removal.

6. Lift the LED assembly from the LCD bezel.

Removing the Pivot Assemblies

Refer to Figures 3-23 through 3-27 for the following steps.

1. Separate the display from the base unit, as explained in the "Separating the Display from the Base Unit" section.

2. Remove screw A with its washer and screw B from each retainer on the display assembly, as shown in Figure 3-23.

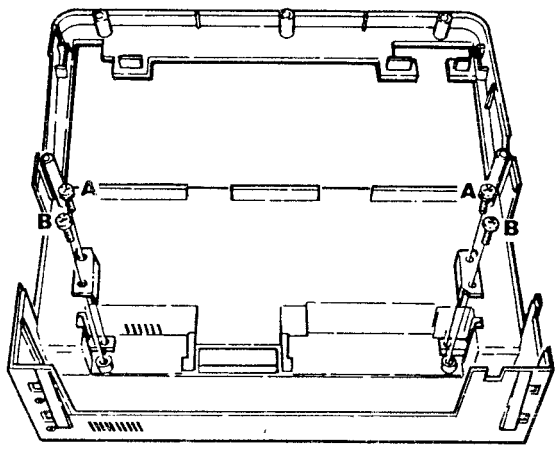


Figure 3-23. Retainer Screws

3. Turn the display assembly over and rotate it from the computer top so the display is open all the way, as shown in Figure 3-24.

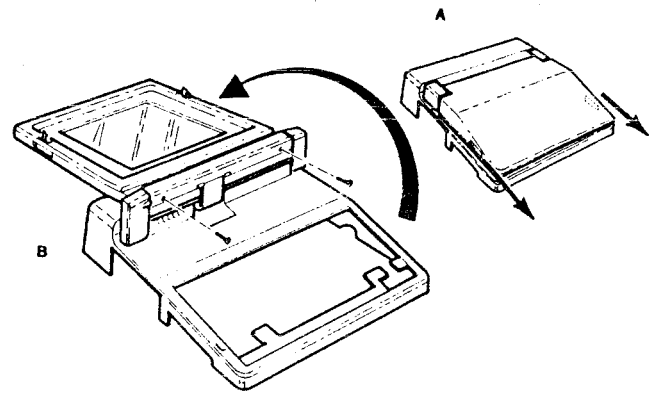


Figure 3-24. LCD Bezel Screws

4. Remove the two screws from the LCD bezel, as shown in Figure 3-24.

5. Separate the LCD bezel from the top cover. Locate the wire coming from the shield to the controls assembly, as shown in Figure 3-25.

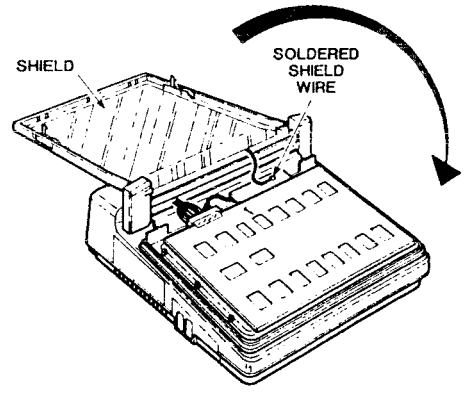


Figure 3-25. Unsoldering the Shield Wire

6. Unsolder the shield wire from the controls assembly and lay the bezel face down, on top of the keyboard. Observe the position of all cables connected to the controls assembly, LED assembly, and LCD assembly so that the cables can be positioned in their original locations during reassembly.

7. Remove the screw securing the left pivot assembly to the display cover, as shown in Figure 3-26. Set the pivot assembly and screw aside.

8. Remove the screw securing the right pivot assembly to the display cover, as shown in Figure 3-26. Set the pivot assembly and screw aside.

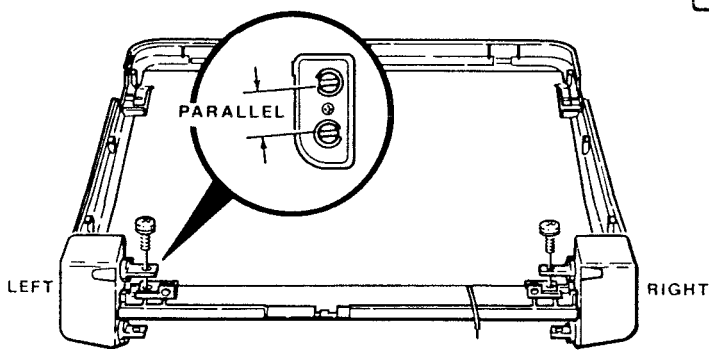


Figure 3-26. Removing the Pivot Assemblies

During reassembly be sure:

- To install the right and left pivots to their respective positions with the flats on the shafts parallel.
- The bottom shaft is in the opening on the base unit top, as shown in Figure 3-26.
- To resolder the shield ground wire.

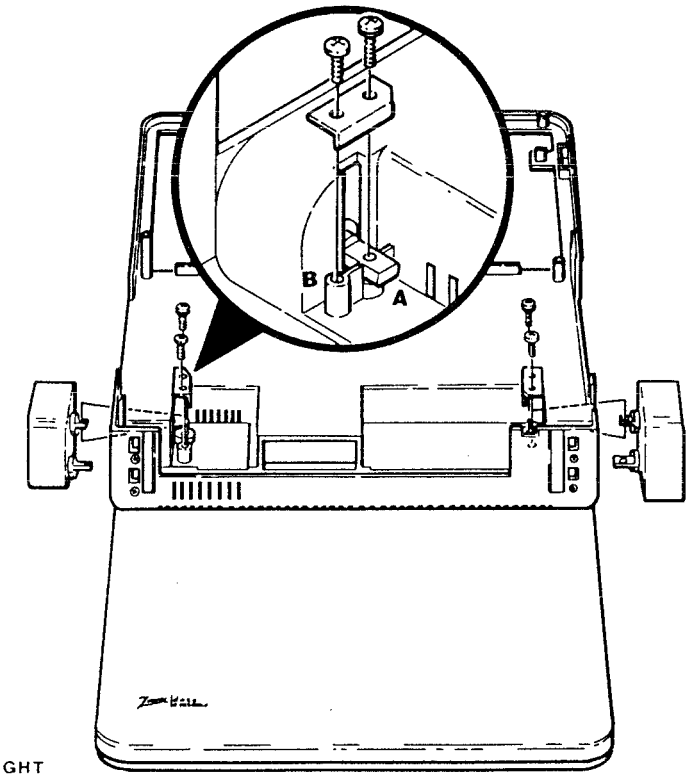


Figure 3-27. Installing the Pivot Assemblies

Removing the Cover Latches

Refer to Figure 3-28 for the following steps.

1. Open the display, as explained in "Opening the Display" section.

2. Remove the screw securing the left latch assembly, as shown in Figure 3-28. Set the latch assembly and screw aside.

3. Remove the screw securing the right latch assembly, as shown in Figure 3-28. Set the latch assembly and screw aside.

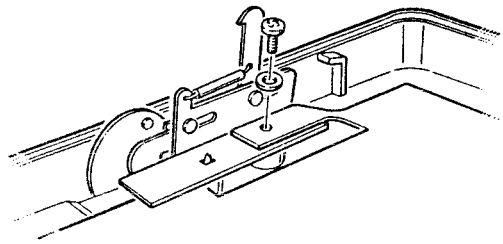


Figure 3-28. Latch Screws

During reassembly, make sure the screws pass through the hole in the shield
first.

Removing the Access Door

Refer to Figure 3-29 for the following steps.

1. Turn off power and disconnect all peripherals.
2. Place the computer face down on a clean soft surface.
3. Remove the access door from the computer by lifting the door at the notch and pulling its tabs free, as shown in Figure 3-29.

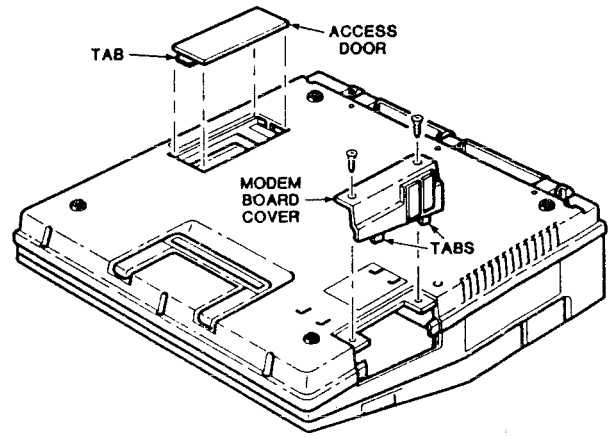


Figure 3-29. Removing the Access Door and the Modem Board Cover

Removing the Modem Board Cover

Refer to Figure 3-29 for the following steps.

1. Turn off power and disconnect all peripherals.
2. Place the computer face down on a clean soft surface.
3. Remove the two screws securing the modem board cover to the computer, as shown in Figure 29.

During reassembly, make sure the modem board cover tabs are on the inside of the base unit bottom.

Chapter 4
Configuration

This chapter describes the Setup/Configuration menu and the display font selection jumpers used in this computer.

Setup/Configuration Menu

The Setup/Configuration menu serves as a reference for the computer by storing information about its configuration in a special CMOS memory device.The information must be changed if you alter the computer's configuration. To run the program, press the CTRL-ALT-INS key combination to drive the computer to the Monitor program. Type SETUP at the Monitor prompt (-->) and press ENTER.

The Setup/Configuration menu display consists of two screens. One displays the hardware information when the computer is used as a portable, that is, when the optional expansion chassis is not attached to the computer. This screen displays the message `Expansion Chassis Not Installed`. The other screen displays hardware information when the optional expansion chassis is attached. This screen displays the message `Expansion Chassis Installed`. You can change from one screen to the other with the Fn-PgUp and Fn-PgDn keys. Each screen may contain different information.

When the Setup/Configuration program screen appears, the active selection in each field is highlighted with a rectangular, reverse-video image, as shown in Figure 4-1.

Use the cursor control keys to move to the fields in the menu. Use the space bar and BACK SPACE key to move between entries within each field, except the time, date, Wini Powerdown, and Backlight fields. These fields must be typed in and entered using the ENTER key..To make a selection in the remaining fields, move to the desired field and highlight the entry that describes the computer. The selection will be locked in when you move to the next field. The message area at the bottom of the screen will provide help and error messages.

Figure 4-1 shows the default, or factory set, entries for the `Expansion Chassis Not Installed` screen. The default entries for the `Expansion Chassis Installed` screen are the same. However, each screen can contain different entries.

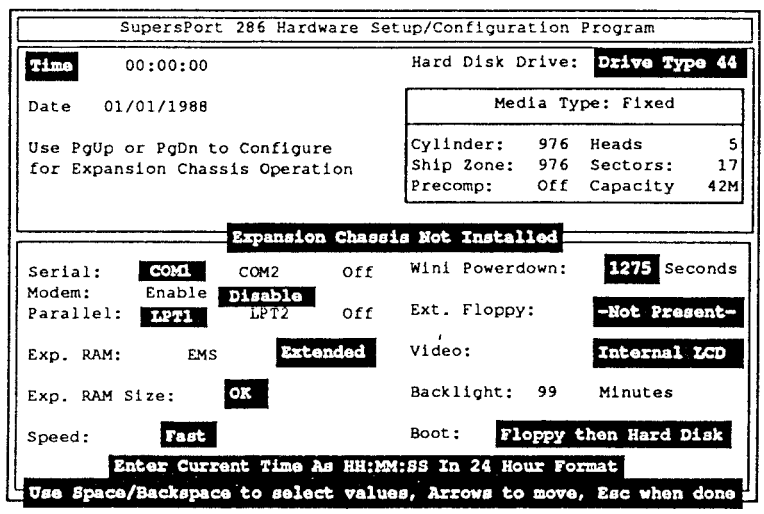

SupersPort 286 Hardware Setup/Configuration Program
Time 00:00:00
Date 01/01/1988
Use PgUp or PgDn to Configure
for Expansion Chassis Operation
Hard Disk Drive: Drive Type 44
Media Type: Fixed
Cylinder: 976 Heads 5
Ship Zone: 976 Sectors: 17
Precomp: Off Capacity 42M
Expansion Chassis Not Installed
Serial: COM1 COM2 Off
Modem: Enable Disable
Parallel: LPT1 LPT2 Off
Exp. RAM: EMS Extended
Exp. RAM Size: OK
Speed: Fast
Wini Powerdown: 1275 Seconds
Ext. Floppy: -Not Present-
Video: Internal LCD
Backlight: 99 Minutes
Boot: Floppy then Hard Disk
Enter Current Time As HH:MM:SS In 24 Hour Format
Use Space/Backspace to select values, Arrows to move, Esc when done

Figure 4-1. Setup/Configuration Menu Screen

The computer's clock and calendar are battery-operated and will run continuously, even when the computer is turned off. To keep accurate time, you must set the time and date when you turn on the computer for the first time. After that, you only need to enter a new time and date if you replace the backup battery.

Time

The computer keeps track of time using a 24-hour clock, in hours (00-23), minutes (00-59), and seconds (00-59). Type in the time of day using this format, and then press the ENTER key. For example, to enter 8:35 a.m., type 083500; to enter 8:35 p.m. type 203500. The computer automatically adds the colons (:) to separate the hours, minutes, and seconds.

If you make a mistake while typing, use the BACKSPACE key to erase the incorrect entry, type it again, and then press the ENTER key.

Date

The computer keeps track of the date using months (1-12), days (1-31), and years. Type in the date using this format, then press the ENTER key. For example, to set the calendar for January 5, 1988, type 01051988. The computer automatically adds the slashes (/) to seperate the month, day, and year.

Again, if you make a mistake while typing, use the BACKSPACE key to erase the incorrect entry, type it again, and then press the ENTER key.

Hard Disk Drive

When the computer is shipped from the factory, the hard disk drive type is set to match the drive that was installed in the computer. You should not change this selection unless the original drive is replaced by a drive of a different type. If the backup battery is replaced, the drive type will have to be re-entered. Press the spacebar to step through the drive types.

Serial

The serial port can be addressed as either COM1 or COM2. If there is no serial device attached to the computer, the serial port can be turned off. Setting the serial port off conserves power during battery operation.

Modem

The modem, if present, can be enabled or disabled. Disabling the modem conserves power during battery operation.

Parallel

The parallel field determines whether the parallel port is addressed as LPT1 or LPT2. Turning the parallel port off conserves battery power.

Expansion RAM

The Expansion RAM field determines whether the expansion memory will be used as EMS memory or extended memory.

Expansion RAM Size

If your computer contains more than 1 megabyte of memory, you need to select the number of kilobytes of expansion memory you have added to the system. The selection ranges from 0K (zero kilobytes) to 15,360K. Use the space bar to increase the number and the BACKSPACE key to choose a lower number. If you do not have any expansion memory, select 0K.

Speed

You have a choice of three speed modes: slow, fast, and smart. The fast speed is the normal (and default) mode of operation. However, some programs

may require a slower speed in order to run. The smart mode slows the computer down for floppy disk drive operations but allows the fast speed for other operations. If the program still does not run properly, it may require the slow mode. This mode slows down all CPU and Memory operations of the computer. Bus speed remains fixed at 6MHz, fast or slow. The slow mode provides the maximum power conservation during battery operation.

Wini Powerdown

This field allows you to set the amount of time the hard disk will continue to spin after the last disk activity. Setting the value to 0 turns the hard disk off while setting this value to the maximum (1275 seconds) causes the hard disk to remain on continuously.

Ext. Floppy

This field is used to identify what type of external floppy disk drive is attached to the computer: 5-1/4 inch 360K, 5-1/4 inch 1.2M, 3-1/2 inch 720K, or 3-1/2 inch 1.4M.

Video

The Video field allows you to choose between the built-in LCD or an external monitor attached to the video connector on the back panel. If the optional expansion chassis is attached to the computer, there are four additional selections available:

Color Card: 40x25 — This settings displays text at 40 characters per line, 25 lines per screen.

Color Card: 80x25 — This setting displays text at 80 characters per line, 25 lines per screen.

Mono Card: 80x25 — This setting selects a high-resolution monochrome display.

Enhanced Graphics — This setting selects an EGA or a high-resolution analog display.

Backlight

Use the Backlight field to set the time the backlight remains lit when there is no activity on the keyboard. Setting this value to 0 (zero) turns the backlight off. Setting the value to 99 (maximum) causes the backlight to remain on continuously. Turning the backlight off conserves power during battery operations.

Boot

The Boot field allows you to select the drive your computer will attempt to boot from when it autoboots. You can select any of the following options:

Floppy Drive 0 — The computer will attempt to load the operating system from the floppy disk drive.

Hard Disk Drive 0 — The computer will attempt to load the operating system from the hard disk drive.

Floppy then Hard Disk — The computer will attempt to load the operating system from the floppy disk drive. If that drive is not ready, the computer will attempt to load the operating system from the hard disk drive.

Enter MFM-200 Monitor — This selection defeats autoboot. The computer will not attempt to load the operating system from either drive but will call up the Monitor program instead.

Display Character Font Selection

The SupersPort 286 computer is capable of displaying several other character sets other than the standard English. The selection of these fonts are controlled by jumpers located near the numeric coprocessor socket.

NOTE: ROM version V1.0 does not support different fonts.

To select a different font:

1. Turn the computer off. If the external AC power supply is attached to the computer, disconnect it.
2. Close and latch the lid.
3. Place a soft cloth on your work surface and turn the computer upside down on the cloth.
4. Carefully pry up on the coprocessor cover, as shown in Figure 4-2.
5. Table 4-1 lists the jumper settings for the various fonts. Set the jumpers according to this list for the desired font. To set a jumper to "0," place the jumper on the two pins toward the end marked "0." To set a jumper to '1," place the jumper on the two pins toward the end marked "1."
6. Replace the cover.

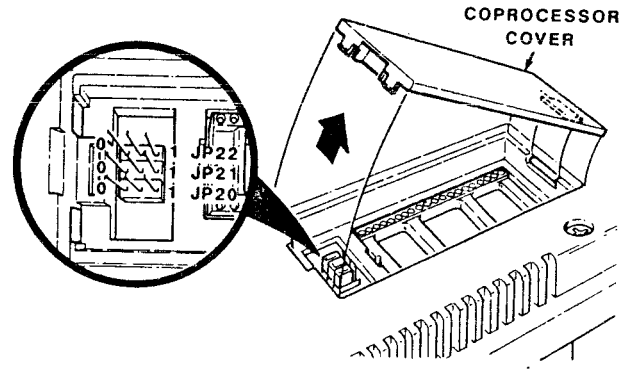


Figure 4-2. Removing the Coprocessor Cover

Table 4-1. Display Font Jumper Settings

JUMPER			
20	J21	J22	LANGUAGE
0	0	0	English
0	0	1	Norwegian
0	1	0	Turkish
0	1	1	Greek
1	0	0	Hebrew
1	0	1	English
1	1	0	English
1	1	1	Reserved

Chapter 5

Circuit Descriptions

In addition to the power supply, the computer contains four major sections, as shown in Figure 5-1: processor, control, memory, and peripheral support. Each of these sections contain a number of major integrated circuits.

The processor section consists of the CPU (80C286), an optional numeric processor extension (80287), and the support integrated circuits. All the calculations and sophisticated processing take place in the CPU and numeric data coprocessor. The support ICs use the signals generated by the CPU and coprocessor to cause other sections of the computer to function.

The control section contains three major integrated circuits that control the operation of the computer: the bus controller, the system control processor (SCP), and the decoder gate array.

The memory section contains the computer's ROM, RAM, and a memory controller. The ROM contains the Monitor program, which provides a number of capabilities. There are two sections of RAM: scratchpad memory, used by the CPU for intermediate calculations and for temporary storage space; and contiguous memory, which provides 1M of user RAM, expandable to 3M.

The peripheral support section consists of the video controller circuitry, parallel and serial communications, mass storage, and the keyboard. These areas are discussed individually in this chapter.

Processor Section

There are four circuit groups in the processor section of the computer:

- The clock circuits, which are necessary to run the CPU and numeric data coprocessor and perform system timing functions.
- The control circuits, which include the interrupt controller, programmable interval timer, and real time clock circuitry.
- The addressing circuits, which allow memory and various input/output devices and ports to be accessed.
- The data circuits, which pass data to and from the various parts of the computer.

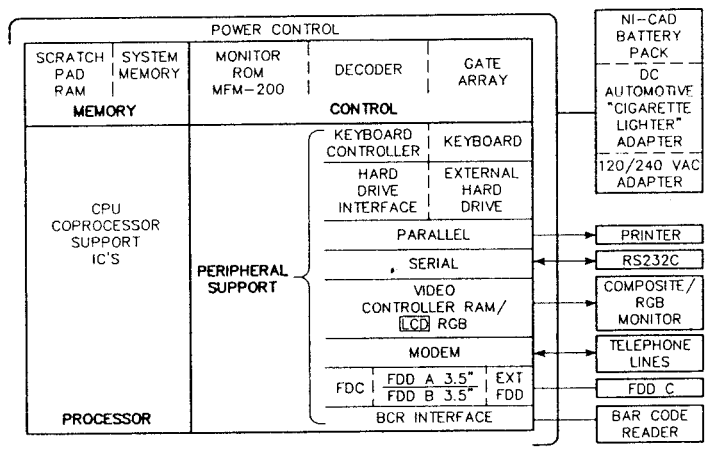


Figure 5-1. Major Circuit Sections

Major Integrated Circuits

The major ICs in the processor section of the computer are:

- The 80C286 CPU
- An optional 80287 numeric coprocessor
- The 82C215 address/data buffer
- The 82C206 peripheral controller

The following sections describe the operation of these integrated circuits.

80C286 CPU

This computer uses the 80C286 microprocessor with a 16-bit data bus and a 24-bit address bus. The 80C286 can also operate within an 8-bit architecture. It exercises all of the functions of a typical 8-bit microprocessor (8088) at an increased rate. Table 5-1 defines the pin functions and Figure 5-2 shows the pinout of the 80C286 microprocessor.

Table 5-1. 80C286 Microprocessor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	$\overline{BHE}$	This output indicates transfer of data on bits D8 - D15. Byte-oriented devices residing on bits D8 - D15 use $\overline{BHE}$ to condition chip select functions.
2, 3	NC	These pins are not connected.
4, 5	$\overline{S1}$, $\overline{S0}$	CPU status lines that distinguish between read and write operations.
6	$\overline{PEACK}$	The 80C286 asserts the $\overline{PEACK}$ signal to acknowledge $\overline{PEREQ}$.
7, 8	A23 - A22	CPU address bits 23 and 22.
9	VSS	Ground
10-28	A21 - A3	CPU address bits 3 through 21.

Table 5-1 (continued). 80C286 Microporcessor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
29	RESET	This input causes a system reset to clear the internal logic of the 80C286 (active-high).
30	VCC	+5 VDC power supply.
31	CLK	System clock. This signal provides fundamental timing for the operation of the 80C286.
32-34	A2 - A0	CPU address bits 0 through 2.
35	VSS	Ground.
36-51	D0 -D15	CPU data bits 0 through 15.
52	CAP	A 0.047 µF capacitor must be connected between this pin and ground to filter the output of the internal bias generator.
53	$\overline{ERROR}$	Numeric processor extension error. Tied high in this computer.
54	$\overline{BUSY}$	Numeric processor extension busy. An active $\overline{BUSY}$ signal causes the 80C286 to stop its program execution if the WAIT instruction or some ESC instructions are received.
57	INTR	Interrupt request. This line conducts interrupt requests to the 80C286, which cause it to suspend its current program execution and enter an interrupt service routine.
59	NMI	Non-maskable interrupt.
60	VSS	Ground.
61	$\overline{PEREQ}$	Processor extension request. When $\overline{PEREQ}$ is high, the 80287 request the 80C286 to allow it to assume program execution for a numeric operation.

Table 5-1 (continued). 80C286 Microporcessor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
62	VCC	+5 VDC power supply.
63	$\overline{\text{READY}}$	Bus ready. When high, bus cycles are extended without limit. The bus cycle terminates once this line is forced low again.
64	HOLD	Hold. This active high input allows the bus controller to request control of the system bus.
65	HOLDA	Hold acknowledge. This output signal informs the bus controller that its request for control of the system bus has been granted.
66	COD/$\overline{\text{INTA}}$	Not connected.
67	M/$\overline{\text{IO}}$	Memory or input/output select. CPU status line that distinguishes between memory and input/output operations.
68	$\overline{\text{LOCK}}$	Not connected.

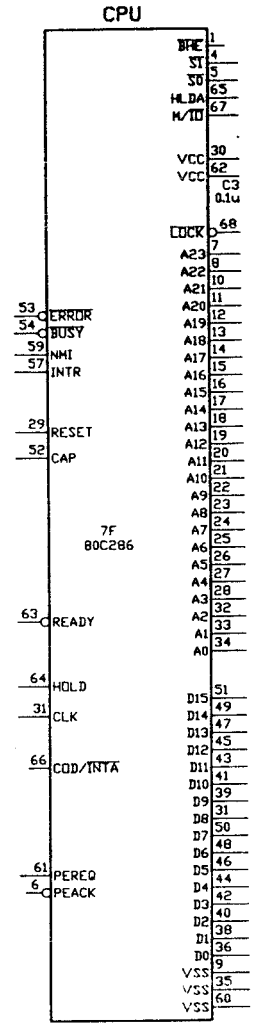


Figure 5-2. 80C286 Microprocessor Pinout

Optional 80287 Numeric Processor Extension

An 80287 numeric processor extension may be installed in the computer as an option. The instruction set for the 80287 contains over fifty additional instructions and its architecture allows it to perform complex mathematical operations with fewer instructions. The 80C286 can perform all of the operations of the 80287 but requires many more machine cycles for each operation. Table 5-2 defines the pin functions and Figure 5-3 shows the pinout of the 80287 numeric processor extension.

Table 5-2. 80287 Numeric Processor Extension Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1-4	NC	Not connected.
5-8	D12-D15	CPU data bits 12 through 15.
9	VCC	+5 VDC power supply.
10	VSS	Ground.
11, 12	D10-D11	CPU data bits 10 and 11.
13	NC	Not connected.
14-23	D0-D9	CPU data bits 0 through 9.
24	PEREQ	Processor extension request. This request indicates to the 80C286 that the 80287 is ready to execute a numeric operation.
25	$\overline{\text{BUSY}}$	80287 busy. This signal indicates to the 80C286 that the 80287 is currently executing a command.
26	$\overline{\text{ERROR}}$	This signal indicates that an unmasked error condition exists.
27	$\overline{\text{NPRD}}$	Numeric processor read. This signal enables transfer of data from the 80287.

Figure 5-2 (continued). 802 Numeric Processor Extension Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
28	$\overline{\text{NPWR}}$	Numeric processor write. This signal allows transfer of data to the 80287.
29	CMD0	Command line 0. This command line, with command line 1, $\overline{\text{NPS1}}$, and NPS2, allows the 80C286 to direct operations to the numeric processor.
30	VSS	Ground.
31	CMD1	Command line 1. This command line, with command line 0, $\overline{\text{NPS1}}$, and NPS2, allows the 80C286 to direct operations to the numeric processor.
32	CLK	This clock input provides the fundamental timing for internal 80287 operations.
33, 34	NPS2	Numeric processor select signals.
	$\overline{\text{NPS1}}$	If $\overline{\text{NPS1}}$ is low and NPS2 is high, the 80287 can perform floating point instructions.
35	RESET	80287 reset. This signal causes the 80287 to terminate its current program execution and enter a dormant state.
36	$\overline{\text{PEACK}}$	This signal acknowledges to the 80287 that its request signal (PEREQ) has been recognized. If there are no more numeric operations pending, the request signal will be withdrawn.
39	CKM	This signal is tied low in this computer.
40	NC	Not connected.

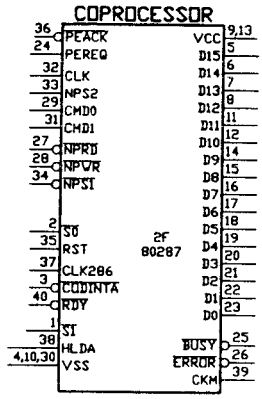


Figure 5-3. 80287 Numeric Processor Extension Pinout

82C215 Address/Data Buffer

The 82C215 address/data buffer incorporates bus conversion logic for 8-bit and 16-bit data transfers. It consists of address buffers and latches, data buffers and latches, and parity generation/detection circuits. However, this computer does not check parity.

The address buffers and latches connect the A1-A16 data bus to the XA1-XA16 data bus. The A1-A16 address lines are latched when the IALE signal is active. The 82C215 generates the XA1-XA16 address lines when the HLDA signal is inactive.

The data buffers and latches connect the D0-D15 data bus to the MD0-MD15 memory data bus. Data direction control is provided through the data read ($\overline{DRD}$) signal, the CPU hold acknowledge signal (HLDA), and the status of the action codes provided by the 82C211 bus controller. 8-bit or 16-bit read operations can be performed in conjunction with these signal states.

Table 5-3 lists the pin descriptions of the 82C215 Data/Address Buffer and Figure 5-4 is an illustration of the pinout.

Table 5-3. 82C215 Address/Data Buffer Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	VSS	Ground.
2,4,6,8	D15-D12	Data line 15 - data line 12. These are the CPU data lines 15 through 12.
3,5,7,9	D7-D4	Data line 7 - data line 4. These are the CPU data lines 7 through 4.
10	XA0	X address line 0. This is address line 0 of the peripheral address bus.
11	$\overline{XBHE}$	Byte high enable. This active low input from the CPU is used to enable high byte parity checking.
12-13	AC1-AC0	Action code 1 - action code 0. These input lines from the 82C211 bus controller are used to control the buffers in the 82C215.
14	$\overline{ACEN}$	Action code enable. This active low input from the 82C211 bus controller validates AC1 and AC0.
15	IALE	Internal address latch enable. This input line is used to latch the CPU address lines on to the X address lines.
16,18,20	D11-D9	Data line 11 - data line 9. These are the CPU data lines 11 through 9.
17,19,21	D3-D1	Data line 3 - data line 1. These are the CPU data lines 3 through 1.
22	VSS	Ground.
23	D8	Data line 8. This is the CPU data line 8.
24	D0	Data line 0. This is the CPU data line 0.

Table 5-3 (continued). 82C215 Address/Data Buffer Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
25-31	A1-A7	Address line 1 - address line 7. These are the system address lines 1 through 7.
32	VDD	+5 VDC.
33-41	A8-A16	Address line 8 - address line 16. These are the system address lines 8 through 16.
42	VDD	+5 VDC.
43	VSS	Ground.
44-52	XA16-XA8	X address line 16 - X address line 8. These are the peripheral address bus lines 16 through 8.
53	HLDA1	Hold acknowledge 1. This input is used to control address and data direction during DMA cycles.
54-60	XA7-XA1	X address line 7 - X address line 1. These are the peripheral address bus lines 7 through 1.
61	MD0	Memory data line 0. This is the memory data bus line 0.
62	MD8	Memory data line 8. This is the memory data bus line 8.
63	MD1	Memory data line 1. This is the memory data bus line 1.
64	VSS	Ground.

Table 5-3 (continued). 82C215 Address/Data Buffer Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
65,67,69, 71,73	MD9-MD13.	Memory data line 9 - memory data line 13. These are the memory data bus lines 9 through 13.
66,68,70, 72	MD2-MD5	Memory data line 2 - memory data line 5. These are the memory data bus lines 2 through 5.
74	$\overline{\text{DRD}}$	Data read. This active low input is used to transfer data from the memory data bus to the CPU data bus.
75	VSS	Ground.
76	DLE	Data latch enable. This input enables the local memory data buffer latch.
77-78	MP0-MP1	Memory parity bit 0 - memory parity bit 1.
79,81	MD6-MD7	Memory data line 6 - memory data line 7. These are the memory data bus lines 6 and 7.
80,82	MD14-MD15	Memory data line 14 - memory data line 15. These are the memory data bus lines 14 and 15.
83	$\overline{\text{PARERR}}$	Parity error. This active low output line signals a non-maskable interrupt to the CPU when the 82C215 detects a parity error.
84	VDD	+5 VDC.

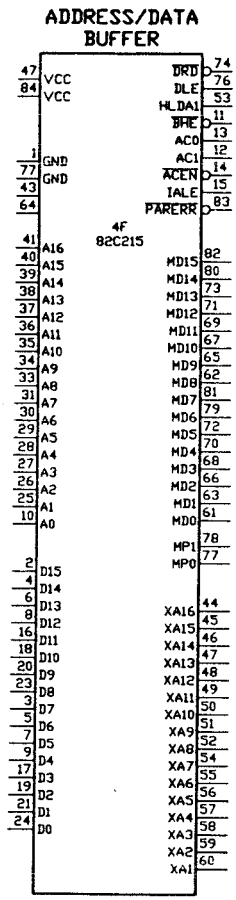


Figure 5-4. 82C215 Address/Data Buffer Pinout

82C206 Integrated Peripherals Controller

The 82C206 integrated peripherals controller (IPC) incorporates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 interval timer, and one MC146818 real time clock all on a single integrated circuit.

DMA controllers — Direct memory access (DMA) speeds the transfer of data from one memory location, device, or peripheral to another. The primary advantage of DMA is in moving blocks of data. The DMA controller has hardware instructions that operate much faster than the software-based CPU instructions. The 82C206 has the equivalent of two 8237 DMA controllers.

Interrupt controllers — The interrupt controllers in the 82C206 accept requests from peripherals, resolve priority on pending interrupts and issue an interrupt request to the CPU. These include interrupts from the timer, keyboard, real-time clock, coprocessor, and input/output ports.

The design of the interrupt controllers on the 82C206 IPC is compatible with the 8259 interrupt controller. Each controller can manage up to eight separate request lines. Since the interrupt controllers are designed in cascade mode, the slave controller uses one line as an input to the master controller. This provides a total of 15 separate interrupt lines that the system can use.

Programmable Interval timer — The programmable interval timer (PIT) on the 82C206 generates time delays and eliminates the need for software timing loops that are subject to such variables as CPU clock speed and interrupt service routines. The PIT contains three 16-bit counters which operate independently of each other. Each counter can be programmed to operate as a timer or a counter.

Real-time clock — The 82C206 includes an internal real-time clock to maintain the system time and date. It also automatically tracks the end-of-month, leap years, and daylight saving time. The internal 100-year calendar ensures accurate date recording for the life of the computer.

Table 5-4 lists the pin descriptions of the 82C206 integrated peripherals controller and Figure 5-5 is an illustration of the pinout.

Table 5-4. 82C206 Integrated Peripherals Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1-3	IRQ5-IRQ3	Interrupt request 5 - interrupt request 3. These asynchronous input lines request an interrupt when they are asserted high. They are held in that state until the first interrupt acknowledge signal is received from the CPU.

Table 5-4 (continued). 82C206 Integrated Peripherals Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
4	IRQ1	Interrupt request 1. This asynchronous input line requests an interrupt when it is asserted high. It is held in that state until the first interrupt acknowledge signal is received from the CPU.
5-11	A23-A17	Address line 23 - address line 17. These system address lines are used by the 82C206 as the upper 7 bits of the DMA page register.
12	GND	Ground.
13	XA16	X Address line 16. This address line is used as the least significant bit of the DMA page register.
14	PWRGD	Power good. This pin is connected to the $\overline{\text{RESET1}}$ line generated by the power supply. When $\overline{\text{RESET1}}$ is high, the CPU is allowed access to the real time clock. When $\overline{\text{RESET1}}$ is low, all address, data, and read/write pins are disconnected from the CPU.
15	PSRSTB	This input establishes the condition of the control registers on power-up. It is tied to the backup battery input line.
16	$\overline{\text{INTA}}$	Interrupt acknowledge. This input signal from the bus controller enables the 82C206 to place interrupt vector data on the data bus.
17	TEST	Test. This pin is tied low and is not used in this computer.

Table 5-4 (continued). 82C206 Integrated Peripherals Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
18	RESET	Reset. This pin clears registers in the DMA and interrupt controllers, assigns IRQ0 the highest priority, sets the slave interrupt controller address, and disables special mask mode in the interrupt controllers.
19	OUT2	Timer 2 output. This pin drives the speaker.
20	OUT1	Timer 1 output. This timer output is a programmed signal for the interrupt request refresh cycles.
21	SCLK	Clock input. This clock generates the timing signals for DMA operations.
22	GATE2	Counter 2 gate input. This signal is used to generate the speaker tone.
23	TMRCLK	Timer clock. Clock input for timers 0 - 2.
24-31	XD7-XD0	X data bus line 7 - X data bus line 0. These are bi-directional data lines connected to the system data bus.
32	VCC	+5 VDC.
33	$\overline{\text{ACK}}$	Acknowledge. When this pin is high, it enables the chip select function for one of the following: DMS controller, DMA page register, interrupt controller, timer, real time clock, or the configuration register. When this pin is low, the 82C206 is essentially disconnected from the system bus.

Table 5-4 (continued). 82C206 Integrated Peripherals Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
34-43	XA9-XA0	X address bus line 9 - X address bus line 0.
44-47	DREQ0-DREQ3	DMA request channel 0 - DMA request channel 3. These input lines are used by peripherals to request DMA service.
48-51	DACK0-DACK3	DMA acknowledge 0 - DMA acknowledge 3. These output lines are used to inform a peripheral that it has been granted a DMA access.
52	$\overline{\text{XIOW}}$	I/O Write. This is a control signal used by the CPU to load information into the internal registers of the 82C206.
54	$\overline{\text{XIOR}}$	I/O read. This is a control signal used by the CPU to read the internal registers of the 82C206.
55-57	DACK7-DACK5	DMA acknowledge 7 - DMA acknowledge 5. These output lines are used to inform a peripheral that it has been granted a DMA access.
58-60	DREQ7-DREQ5	DMA request channel 7 - DMA request channel 5. These input lines are used by peripherals to request DMA service.
61	$\overline{\text{DMAMEMR}}$	DMA memory read. During DMA read or memory-to-memory transfers, this signal is used to access data from the selected memory location.
62	$\overline{\text{DMAMEMW}}$	DMA memory write. During DMA write or memory-to-memory transfers, this signal is used to write data to a selected memory location.

Table 5-4 (continued). 82C206 Integrated Peripherals Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
63	$\overline{\text{AEN8}}$	Address enable 8. This is the address enable signal for 8-bit DMA transfers. Enables address bits A8 - A15 onto the address bus.
64	$\overline{\text{AEN16}}$	Address enable 16. This is the address enable signal for 16-bit DMA transfers. Enables address bits A9 - A16 onto the system address bus.
65	ADSTB16	Address strobe 16. This line is the address strobe for 16-bit DMA transfers (channels 5 - 7). This signal controls the latching of address byte A9 - A16.
66	ADSTB8	Address strobe 8. This line is the address strobe for 8-bit DMA transfers (channels 0 - 3). Controls the latching of address byte A8 - A15 for 8-bit peripherals.
67	TC	Terminal count. When the terminal count for any channel is reached, except channel 0 in memory-to-memory transfers, the DMA controller will generate a pulse. When the TC pulse occurs, the DMA controller will terminate service.
68	IOCHRDY	I/O channel ready. This signal extends the memory read and write pulses for the DMA controllers to accommodate slow memories or peripherals.
69	HRQ	Hold request. Requests control of the system bus when a DMA request is asserted.
70	INTR	Interrupt. Whenever an interrupt request is asserted, this signal activates and interrupts the CPU.

Table 5-4 (continued). 82C206 Integrated Peripherals Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
71	AS	Address strobe. This signal is used to latch the address from the XD bus.
72	OSCI	Oscillator input. 32.768 KHz time base.
73	HLDA	Hold acknowledge. This signal originates in the CPU and indicates it has turned over control of the system busses.
74	GND	Ground.
75	VCC	+5 VDC.
76-84	IRQ15-1RQ6	Interrupt request 15 - interrupt request 6. These asynchronous input lines request an interrupt when they are asserted high. They are held in that state until the first interrupt acknowledge signal is received from the CPU.

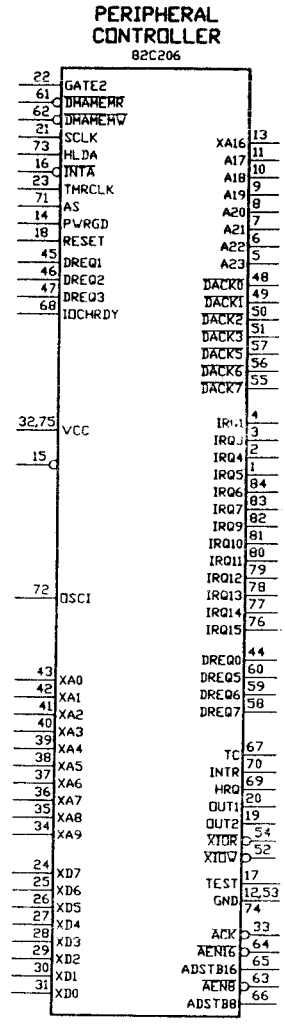


Figure 5-5. 82C206 Integrated Peripherals Controller

Control Section

The control section contains the bus controller and the system control processor. The bus controller provides synchronization and control signals for all the buses in the computer. The system control processor controls communication with the keyboard.

Major Integrated Circuits

The following sections describe the operation of the 82C211 bus controller and the 80C42 system control processor.

82C211 Bus Controller

The 82C211 Bus Controller incorporates speed-selectable clock logic, optional clock logic to drive the AT-bus, interface logic for the CPU, programmable registers for command delays and wait states, and an access register to port 00BH for AT-compatibility.

The reset and automatic shutdown logic monitors the status of the $\overline{\text{RESET1}}$ and $\overline{\text{BRESET2}}$ signals. $\overline{\text{RESET1}}$ is derived from the power supply good (PWRGOOD) signal and $\overline{\text{RESET2}}$ is a "warm" reset provided by the 8742 system control processor. Whenever $\overline{\text{RESET1}}$ is active-low RESET3 and RESET4 are asserted to create a system reset as follows:

During a warm reset, $\overline{\text{RESET2}}$ activates RESET3 which is tied directly to the 80286 CPU. RESET4 will remain active whenever $\overline{\text{RESET1}}$ is active-low and causes the AT-bus, the 82C206 integrated peripherals controller, the system control processor, and the 82C212 memory controller to be reset.

Clock Logic — The clock logic in the 82C211 bus controller operates on two fundamental clock signals. CLK2IN is a TTL-compatible signal that runs at 24 MHz and ATCLK is a XXX MHz signal taken from crystal oscillator XTAL2. Either of these clocks can be chosen as a primary clock source.

Table 5-5 defines the pin functions and Figure 5-6 shows the pinout of the 82C211 bus controller.

Table 5-5. 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	GND	Ground
2	PROCCLK	CPU clock. This signal runs the 80286 CPU and the 82C212 memory controller. The signal is derived from either CLK2IN or ATCLK.
3	NPRST	80287 reset. This active-high signal will reset the 80287 numeric processor. If RESET4 is active the NPRST signal also is active.
4	NPINT	80287 interrupt. This interrupt request is issued by the 80287 and is connected to pin 78 (IRQ13) of the 82C206 IPC.
5	CLK2IN	24 MHz Clock.
6	$\overline{\text{NPCS}}$	80287 chip select. When active-low, the 80287 internal register set is enabled.
7	$\overline{\text{BUSY}}$	80287 busy. When the 80287 begins an arithmetic operation, it asserts this line active-low to inform the CPU.
8	NC	Not used.
9	$\overline{\text{XMEMR}}$	Bus memory read. If the CPU is controlling the bus, this signal is an output to enable memory to place data on the bus. If the DMA circuits control the bus, this signal is an input to the 82C211.
10	$\overline{\text{XMEMW}}$	Bus memory write. If the CPU is controlling the bus, this signal is an output to enable memory to accept data on the bus. If the DMA circuits control the bus, this signal is an input to the 82C211.
11	$\overline{\text{PARERR}}$	Parity error. This computer does not support parity checking.This signal tied high.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
12	$\overline{\text{MEMCS16}}$	16-bit memory chip select. This active-low input indicates that a 16-bit memory transfer is in process. If this line is high, it indicates that an 8- bit memory transfer is enabled.
13	$\overline{\text{RESET1}}$	Reset. This signal is taken from the power supply good signal (PWRGOOD) and is used to activate the RESET3 and RESET4 signals.
14-16	A9 - A7	Address line 9 - address line 7. These address lines are normally generated by the CPU. They are output lines in the 82C211 during refresh cycles.
17	GND	Ground.
18-21	A6 - A3	Address line 6 - address line 3. These address lines are normally generated by the CPU. They are output lines in the 82C211 during refresh cycles.
22	GND	Ground.
23-25	A2 - A0	Address line 2 - address line 0. These address lines are normally generated by the CPU. They are output lines in the 82C211 during refresh cycles. A1 detects CPU shut down conditions and A0 provides the enable signal for the data bus transceivers.
26	HRQ1	Hold request. During a DMA bus cycle this line is asserted active-high by the 82C206 IPC. The 82C211 processes the request and issues a hold request to the CPU.
27	$\overline{\text{AEN1}}$	Address enable 1. This signal is issued by the DMA control circuits to enable 8-bit DMA transfers.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
28	$\overline{\text{AEN2}}$	Address enable 2. This signal is issued by the DMA control circuits to enable 8-bit DMA transfers.
29	XA0	Address line XA0. This line acts as an output during CPU accesses over the XA0-XA15 address bus. During 8-bit DMA cycles this line acts as an input line.
30	$\overline{\text{IOCHCK}}$	I/O channel check. If an error condition occurs during an I/O cycle on the AT-bus, this active-low input causes the 82C211 to issue a non-maskable interrupt to the CPU.
31	IOCHRDY	I/O channel ready. This signal is issued over the AT-bus to indicate I/O channel ready status. If the signal state is low, the I/O channel is not ready and the 82C211 will cause wait states to be added to the current cycle.
32	$\overline{\text{ERROR}}$	Error condition. This signal is issued by the 80287 to indicate that an arithmetic error condition has occurred.
33	$\overline{\text{IOCS16}}$	16-bit I/O channel select. When this signal is active-low it indicates that the current I/O cycle is 16-bits wide. If high, this signal indicates that the current I/O cycle is 8-bits wide.
34	SDIR0	System bus direction 0. When this signal is low it causes data to be passed from the SD0-SD7 bus to the MD0-MD7 bus. When high, it reverses data direction.
35	$\overline{\text{8042CS}}$	SCP chip select. This signal enables the system control processor.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
36	SDIR1	System bus direction 1. When this signal is low it causes data to be passed from the SD8-SD15 bus to the MD8-MD15 bus. When high, it reverses data direction.
37	HOLDA	Hold acknowledge. This signal is issued to the 82C211 by the CPU in response to a hold request. It indicates that the system busses are free.
38	RESET4	Reset. This signal resets the AT-bus, the 82C206 IPC, the system control processor, and the 82C212. It is synchronized with PROCCLK.
39	NMI	Non-maskable interrupt. The 82C211 asserts this line high to initiate a NMI.
40	HLDA1	Hold acknowledge 1. This signal goes high when a bus cycle is granted in response to HRQ1.
41	IALE	Internal address latch enable. This active-high signal is asserted synchronously with PROCCLK to control address latches during bus cycles.
42	VCC	+5 VDC.
43	GND	Ground.
44	ALE	Address latch enable. This signal is synchronized with the AT-bus state machine. It controls the address latches on the AT-bus.
45,46	AC0-AC1	Action codes 0-1. These 2-bit codes set the bus size (8-bit or 16-bit) and byte assembly operations performed by the 82C215.
47	$\overline{\text{ACEN}}$	Action code enable. This signal enables the action code lines (pins 45 and 46) to output code.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
48	$\overline{\text{ROMCS}}$	ROM chip select. In this computer, this signal enables the Monitor ROMs to output data.
49	$\overline{\text{BHE}}$	Byte high enable. When this signal is active-low it enables data transfer over the D8 - D15 data bus. This line is an input during CPU cycles when A0 is valid. This line is an output during DMA cycles when XA0 is valid.
50	RESET3	Reset. Whenever $\overline{\text{RESET1}}$ or $\overline{\text{RESET2}}$ are active they force RESET3 to an active-high state. If a shutdown condition occurs, RESET3 will go high. This line is tied directly to the 80286 reset line.
51	$\overline{\text{RESET2}}$	Reset. This signal is issued by the SCP when a warm reset is called for. It activates the RESET3 signal to reset the CPU.
52	REFREQ	Refresh request. When memory requires refresh, the 82C206 IPC issues the active-high REFREQ signal to the 82C211. The 82C211 processes the request and initiates a memory refresh cycle.
53	TMROUT2	Second timer output. This active-high input is issued by the 8254-compatible timer circuits.
54	$\overline{\text{INTA}}$	Interrupt acknowledge. This signal is issued to the interrupt control circuits in the 82C206 IPC. During an interrupt acknowledge cycle, $\overline{\text{INTA}}$ controls data movement between the XD0-XD15 and SD0-SD15 busses.
55	HOLD	CPU hold request. This signal is active-high for DMA and refresh cycles.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
56	$\overline{\text{XIOW}}$	X bus I/O write. When this signal is active-low it causes data on the XD0-XD15 bus to be written to the specified I/O port. If the CPU controls the bus, this signal is an output. If the DMA circuits control the bus, this signal is an input.
57	$\overline{\text{XBHE}}$	X byte high enable. This active-low signal indicates the data is available on the XD8-XD15 bus. If the CPU controls the bus, this signal is an output. If the DMA circuits control the bus, this signal is an input.
58	$\overline{\text{REF}}$	Refresh. When this signal is an output it initiates a memory refresh cycle. When it is an input it can be used to force a refresh cycle from an I/O device.
59-62	XD7-XD4	X data bus line 7 - X data bus line 4. These are the X data bus lines 7 through 4.
63	VCC	+5 VDC.
64	GND	Ground .
65-68	XD0-XD3	X data bus line 0 - X data bus line 3. These are the X data bus lines 0 through 3.
69	$\overline{\text{0WS}}$	Zero wait states. This active-low input causes the current AT-bus cycle to end.
70	$\overline{\text{XIOR}}$	X bus I/O read. When this signal is active-low it causes data from a specified I/O port to be placed on the XD0-XD15 bus. If the CPU controls the bus this line is an output. If the DMA control circuits control the bus this line is an input.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
71	$\overline{\text{READY}}$	Ready. This output causes the current CPU cycle to end after IOCHRDY goes high and $\overline{\text{0WS}}$ is high, or if a timeout condition occurs. During all other cycles, this line is an input from the 82C212.
72	M/$\overline{\text{IO}}$	Memory or I/O cycle. When the CPU asserts this signal high a memory cycle is enabled. When the CPU asserts this signal low, an I/O cycle is enabled.
73	$\overline{\text{EALE}}$	External address latch enable. This active-low output latches the A17-A23 address lines onto the LA17-LA23 address lines (AT-bus). This signal is used in the delayed mode.
74	$\overline{\text{NPBUSY}}$	80287 busy. The 80287 issues this signal when it begins to execute an arithmetic operation. The 82C211 processes this signal and issues the BUSY signal to the CPU.
75	TMRGATE	Timer gate. This signal enables the counter circuits of the 8254-compatible timer in the 82C206.
76	ATCLK1	AT-bus clock 1. This XXX MHz clock input is used to control the AT-bus. This signal is not required if the AT-bus state machine clock (BCLK) is sourced from the CLK2IN signal.
77	SPKDATA	Speaker data. When this signal is active-high it gates the tone generator signal (from the 8254-compatible circuits) to the speaker. The tone generator signal is output by the 82C206 IPC.

Table 5-5 (continued). 82C211 Bus Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
78	$\overline{AF16}$	Bus cycle type. When this signal is high it indicates that the current bus cycle is a local CPU cycle. When low, it indicates that the current cycle is an AT-bus cycle.
79,80	$\overline{SO}$, $\overline{S1}$	Status lines $\overline{S0}$ and $\overline{S1}$. These lines are used by the 80286 to provide current bus cycle status.
81	ATCLK2	AT-bus clock 2. This output line is connected to crystal oscillator XTAL2. This signal works in conjunction with ATCLK1.
82	ASRTC	Real-time clock address strobe. This signal is issued to the 82C206 to control the real-time clock circuits.
83	SYSCLK	System clock. This clock is used to control the AT-bus I/O channel. In this computer, SYSCLK is one-half the frequency of BCLK.
84	VCC	+5 VDC.

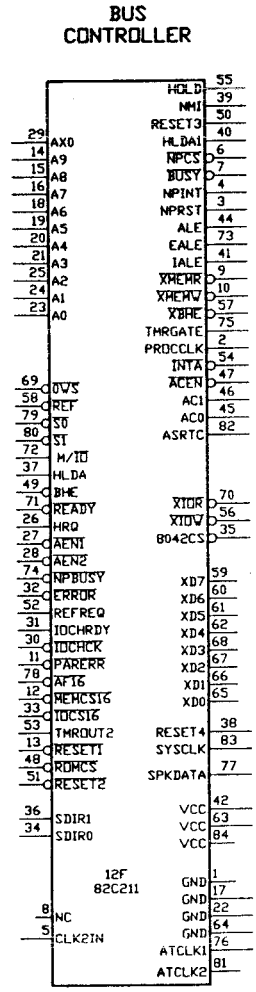


Figure 5-6. 82C211 Bus Controller Pinout

System Control Processor

The system control processor, an 8-bit 80C42 UPI (universal peripheral interface), allows the 80C286 CPU to communicate with the keyboard. The 80C42 is a programmed device that has internal ROM, RAM, I/O ports, and a clock generator. The 80C42 is programmed to handle bidirectional synchronized serial communications with the keyboard. Figure 5-7 illustrates the pinout of the 80C42 and Table 5-6 describes the signals at this device.

Table 5-6. System Control Processor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	T0	Testable input 0. This signal is used to reset the SCP instruction state and synchronize the internal clock. In this computer it is driven by the keyboard clock (KBCLK) signal.
2	XTAL 1	Clock input. In this computer, this signal is gated with respect to the system clock signal (SYSCLK).
3	XTAL 2	Clock input. Provides the processor clock input signal for device timing purposes. In this computer, this signal is gated and inverted with respect to the system clock signal (SYSCLK).
4	$\overline{\text{RESET}}$	Reset. Resets the processor to a known state. In this computer, the $\overline{\text{RESET4}}$ signal is applied to this line.
5	$\overline{\text{SS}}$	Single step. In this computer, this line is pulled high.
6	$\overline{\text{CS}}$	Chip select. An active-low $\overline{\text{8042CS}}$ signal on this pin selects the 80C42 processor.
7	EA	External access. In this computer, this line is connected to ground (disabled).

Table 5-6 (continued). System Control Processor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
8	$\overline{\text{RD}}$	Read. The $\overline{\text{XIOR}}$ signal is applied to this line. It allows the CPU to access the internal status register or the output buffer of the SCP.
9	A0	Command/data select. The CPU uses bit XA2 (applied to this line) to indicate whether the byte being transferred is a command (XA2 = 1) or data (XA2 = 0).
10	$\overline{\text{WR}}$	Write. When The $\overline{\text{XIOW}}$ signal is applied to this line. It allows the CPU to write data or commands to the input buffer of the SCP.
11	SYNC	Not used.
12-19	DB0-DB7	Data bus. 8-bit, tri-state, bi-directional XD0-XD7 data bus.
20	GND	Ground.
21	P20	Port 2, bit 0 (80286 reset). An active-high output signal (RESET2) on this line will reset the CPU.
22	P21	Port 2, bit 1 (A20GATE). The output of this pin will determine the status of the A20 address line. If this bit is set, the A20 address line will function normally. If this bit is low, the A20 line is disabled.
23	P22	Port 2, bit 2 ($\overline{\text{WRTCFG}}$). The SCP asserts the write configuration signal onto this pin. It is used to enable programming operations to the device in the expansion box.
24	P23	Port 2, bit 3 ($\overline{\text{VIDEN}}$). This signal is applied to the decoder gate array to enable/disable the internal LCD video control circuits.
25	PROG	Not used. In this computer, this line is pulled high.

Table 5-6 (continued). System Control Processor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
26	POWER	+5 VDC supply voltage.
27	P10	Not used. In this computer, this line is pulled high.
28	P11	Port 1, bit 1 ($\overline{\text{BZXBUSEN}}$). This signal informs the SCP whether or not the expansion box is connected to the computer. If the signal state is low, the expansion box is present.
29	P12	Port 1, bit 2 ($\overline{\text{MODEMEN}}$). This signal is output to enable external modem operation. Power is applied to the modem when the $\overline{\text{MODEMEN}}$ signal is low.
30	P13	Port 1, bit 3 (FONT). This signal is used in conjunction with the signal on pin 36. They determine the video font for the display. If both pins are low, the font is an 8 x 8 character cell. If both pins are high, the font is an 8 x 16 character cell.
31	P14	Not used. In this computer, this line is pulled high.
32	P15	Port 1, bit 5 ($\overline{\text{LCD}}$/RGB). The status of this signal indicates the type of active video display. When the signal state is low, the LCD display is active. When high, a raster-scan type of display is active.
33	P16	Port 1, bit 16 (BACKLIGHTON). When this signal is high it indicates that the LCD backlight feature is active.
34	P17	Port 1, bit 7 (HDLOW). This signal goes high if the battery pack capacity is too low to support hard disk access.

Table 5-6 (continued). System Control Processor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
35	P24	Port 2, bit 4 (IRQ1). The status of this bit reports the condition of this interrupt line. If the bit is set (1), an interrupt request is active. If the bit is clear (0), no interrupt requests are in process.
36	P25	Port 2, bit 5 (FONT). This signal is used in conjunction with the signal on pin 30. They determine the video font for the display. If both pins are low, the font is an 8 x 8 character cell. If both pins are high, the font is an 8 x 16 character cell.
37	P26	Port 2, bit 6 (KCKOUT). The clock signal used by the system keyboard is output on this pin.
38	P27	Port 2, bit 7 (KDTOUT). Data transmitted to the keyboard is sent via this pin.
39	T1	Keyboard data (KBDATA). This line carries keyboard data generated by the keyboard interface controller. The SCP outputs data to the keyboard through pin 38.
40	GND	Ground. System ground connection.

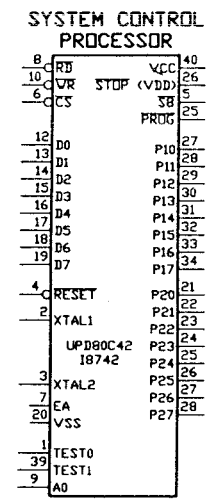


Figure 5-7. System Control Processor Pinout

Memory Section

The computer's communication with memory is handled by the 82C212 memory controller. The 82C212 uses a page/interleave mode of operation. In this mode, memory is organized into two 16-bit banks with even word addresses on one bank and odd word addresses on the other bank. Each bank contains four 256 x 4-bit memory chips. There are no parity bits.

Page/interleave operation makes it possible to achieve zero wait state operation at 12 MHz using 150 ns DRAMs. Zero wait state access between the two banks is accomplished by overlapping $\overline{CAS}$ precharge time of one bank with $\overline{CAS}$ active time of the other bank. The DRAM $\overline{RAS}$ line for both banks are held active until the $\overline{RAS}$ active time out period, at which time a $\overline{RAS}$ precharge for that bank is required.

The Monitor ROM is a read-only memory device that contains the Monitor program, self-tests, initialization routines, and BIOS.

The scratchpad memory is used by the Monitor program to temporarily store intermediate information used by the CPU and operating system.

Major Integrated Circuits

The major integrated circuits in the memory section include the 82C212 memory controller, Monitor ROM, and 1M of user memory.

The 82C212 Memory Controller

The 82C212 Page/Interleave and EMS Memory Controller supports interleaved memory access, page-mode memory access, EMS memory, shadow memory, and the OS/2 operating system.

Clock logic — A 14.31818 MHz oscillator provides the OSC and OSC/12 clock signals. The OSC/12 signal supplies the $\overline{RAS}$ timeout clocks for each memory bank. $\overline{RAS}$ goes inactive after the timeout is reached.

ROM and dynamic RAM control logic — When the computer powers up and begins to initialize, the ROM control circuits provide access to the Monitor ROM by asserting the $\overline{ROMCS}$ signal. The CPU reads code from the ROM and begins to execute a memory cycle. The DRAM control circuits provide the row-address strobe ($\overline{RAS}$), column-address strobe ($\overline{CAS}$), and memory write enable ($\overline{MWE}$) signals required for access to dynamic memory. If wait states are required for the access they are inserted accordingly. After each memory cycle the 82C212 issues the $\overline{READY}$ signal to the CPU.

System control logic — The 82C212 generates the X-bus data enable signal ($\overline{XDEN}$), the data latch enable signal (DLE), the data read signal ($\overline{DRD}$), and the bus cycle type signal ($\overline{AF16}$). $\overline{XDEN}$ controls data gating between the XD0-XD7 bus and the MA0-MA7 address lines. When the address is valid and $\overline{XDEN}$ is active the 82C212 internal register set is enabled. The DLE signal controls data direction between the CPU data bus (D0-D15) and the memory data bus (MD0-MD15). The $\overline{DRD}$ signal enables a read operation from the MA0-MA15 bus to the D0-D15 bus. The bus cycle type signal ($\overline{AF16}$) is asserted during all local memory cycles.

Memory mapping — The 82C212 memory controller supports many different memory configurations through various memory mapping registers. This computer contains 1 megabyte of contiguous DRAM on the main board. The first 640K address space (000000H - 09FFFFH) contains user-addressable memory and the next 360K address space (0A0000H - 0FFFFFH) is reserved for ROM code, scratch pad memory, EMS frame address space, and shadow RAM.

Shadow RAM control — When this computer initializes at power-up it downloads its BIOS to dynamic RAM at address space F1000H - 0FFFFFH. The BIOS then jumps down to shadow RAM, write-protects itself, and continues execution from shadow RAM. By running BIOS from dynamic RAM, the routines execute much faster.

EMS address logic — The EMS address logic allows dynamic memory above the 1 megabyte boundary to be accessed through the system RAM address range 0D000H - 0DFFFFH.

The 82C211 provides address translation to allow access to any 64K segment of DRAM between the 1 megabyte and 2 megabyte address range (this computer supports a maximum of 2 megabytes). Address lines A14-A22 provide the actual addresses so it is not necessary to shift the CPU into protected mode.

Refresh Logic — During refresh, valid refresh addresses are generated on the A0-A9 bus by the 82C211 bus controller. The active-low $\overline{REF}$ signal is issued to the 82C212 which in turn generates refresh addresses on the MA0-MA9 bus. The 82C212 also provides the $\overline{RAS}$ signal and the low megabyte chip select signal ($\overline{LMEGCS}$).

Table 5-7 describes the pin functions of the 82C212 Memory Controller and Figure 5-8 is an illustration of the pinout.

Table 5-7. 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	VSS	Ground.
2-8	A3-A9	Address line 3 - address line 9. These are the CPU address lines 3 through 9.
9-11	A11-A13	Address line 11 - address line 13. These are the CPU address lines 11 through 13.
12	RESET4	Reset. This signal is asserted by the 82C211 bus controller. It causes the 82C212 to set its internal registers to their default values.

Table 5-7 (continued). 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
13	$\overline{ROMCS}$	BIOS ROM chip select. This signal is connected to the output-enable pins of the BIOS ROMs. When active, $\overline{ROMCS}$ allows code to be taken from the ROMs.
14	$\overline{XIOW}$	I/O cycle write. When this signal is active it enables an I/O write cycle to begin.
15	$\overline{XIOR}$	I/O cycle read. When this signal is active it enables an I/O read cycle to begin.
16	$\overline{XMEMW}$	X-bus memory write. This signal enables the 82C212 to direct the appropriate data transceivers to pass data from the X-bus to memory.
17	$\overline{XMEMR}$	X-bus memory read. This signal enables the 82C212 to direct the appropriate data transceivers to pass data from memory to the X-bus.
18	OSC	14.31818 MHz oscillator. This signal is the system clock signal capable of driving .024 amps.
19	HLDA1	Hold acknowledge 1. The 82C211 bus controller generates this signal when a bus cycle is granted by the CPU in response to a DMA hold request. When the 82C212 receives HLDA1 it generates row- and column-address strobe signals for the DMA cycle.
20	$\overline{REF}$	Refresh. The 82C211 bus controller issues this signal for refresh cycles. When the 82C212 receives an active $\overline{REF}$ signal it initiates the refresh cycle.

Table 5-7 (continued). 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
21	OSC/12	1.19 MHz Oscillator. This signal is 1/12 the frequency of the crystal oscillator signal applied to pin 23.
22	GND	Ground.
23	X1	14.31818 MHz crystal input.
24	X2	14.31818 MHz crystal output.
25	$\overline{\text{LMEGCS}}$	Low megabyte chip select. This output is asserted when the address space up to 1 megabyte is active (for memory cycles or refresh cycles). It disables the system memory read/write control (on the AT-bus) when access to memory beyond 1 megabyte is made.
26	$\overline{\text{XDEN}}$	X-bus data buffer enable. This signal enables the buffers between the XD0-XD15 data bus and the MD0-MD15 data bus.
27	$\overline{\text{XDIR}}$	X-bus data direction. This signal controls the direction of data passage between the XD0-XD15 data bus and the SD0-SD15 data bus. When $\overline{\text{XDIR}}$ is low, data is passed to the X-bus. When high, data is passed to the S-bus.
28	$\overline{\text{MWE}}$	Memory write enable. This signal is asserted for write operations during a memory cycle.
29	$\overline{\text{READY}}$	Ready. This signal is an input to the 82C212 during AT-bus cycles and an output for local memory and I/O cycles. Each time a requests memory or I/O data transfer is completed, $\overline{\text{READY}}$ is issued to the CPU.

Table 5-7 (continued). 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
30	A20GATE	Gate address line A20. This line is used for programs that map addressing beyond 1 megabyte into the first 640K of local memory. When inactive, this signal allows the CPU to use address line A20.
31	GA20	Gated address line A20. This signal is the gated status of the A20GATE signal.
32	VCC	+5VDC.
33	$\overline{\text{DRD}}$	Data read. When this signal is low, data is moved from the memory data bus to the local CPU data bus (in the 82C215 buffer). When high, data is moved from the CPU to memory.
34	$\overline{\text{BHE}}$	Byte high-enable. When the CPU transfers data over the D8-D15 segment of the data bus, it issues $\overline{\text{BHE}}$ to the 82C212 to specify the operation.
35	$\overline{\text{CAS30}}$	Column address strobe 30. This signal is used for expansion memory. It selects the low-byte memory devices of memory bank 3 (fourth 512K bank).
36	$\overline{\text{CAS31}}$	Column address strobe 31. This signal is used for expansion memory. It selects the high-byte memory devices of memory bank 3 (fourth 512K bank).
37	$\overline{\text{CAS20}}$	Column address strobe 20. This signal is used for expansion memory. It selects the low-byte memory devices of memory bank 2 (third 512K bank).

Table 5-7 (continued). 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
38	$\overline{\text{CAS21}}$	Column address strobe 21. This signal is used for expansion memory. It selects the high-byte memory devices of memory bank 2 (third 512K bank).
39	$\overline{\text{CAS10}}$	Column address strobe 10. This signal is used for system memory. It selects the low-byte memory devices of memory bank 1 (second 512K bank).
40	$\overline{\text{CAS11}}$	Column address strobe 11. This signal is used for system memory. It selects the high-byte memory devices of memory bank 1 (second 512K bank).
41	$\overline{\text{CAS00}}$	Column address strobe 00. This signal is used for system memory. It selects the low-byte memory devices of memory bank 1 (first 512K bank).
42	VCC	+5 VDC.
43	GND	Ground.
44	$\overline{\text{CAS01}}$	Column address strobe 01. This signal is used for system memory. It selects the high-byte memory devices of memory bank 1 (first 512K bank).
45	DLE	Data latch enable. This signal enables the local memory data buffer in the 82C215 buffer.
46	A10	Address line 10. This is the CPU address line 10.
47	A14	Address line 14. This is the CPU address line 14.
48	A0	Address line 0. This is the CPU address line 0.

Table 5-7 (continued). 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
49-53	A15-A19	Address line 15 - address line 19. These lines are the CPU local address bus lines 15 and 19.
54	M/$\overline{\text{IO}}$	Memory or I/O channel cycle select. When this signal is high, a memory cycle is enabled. When low, an I/O channel cycle is enabled.
55-58	A20-A23	Address line 20 - address line 23. These lines are the CPU local address bus lines 20 and 23.
59	$\overline{\text{AF16}}$	Bus cycle type. This signal is asserted active-low during local memory cycles. It is high for all other cycles.
60-62	MA0-MA2	Multiplexed memory address lines. These lines are used during normal memory cycles to address RAM. They are also used to access the internal registers of the 82C212.
63	$\overline{\text{S0}}$	Status line 0. The 82C212 monitors this line to detect the start of various cycles.
64	GND	Ground.
65	$\overline{\text{S1}}$	Status line 1. The 82C212 monitors this line to detect the start of various cycles.
66-70	MA3-MA7	Multiplexed memory address lines. These lines are used during normal memory cycles to address RAM. They are also used to access the internal registers of the 82C212.

Table 5-7 (continued). 82C212 Memory Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
71,72	MA8,MA9	Multiplexed memory address lines. These lines are used during normal memory cycles to address RAM. They are also used to access the internal registers of the 82C212.
73	DLY0	Delay 0. This delayed signal is used with DLY1 and DLY2 to generate memory control signals.
74	A1	Address line 1. This is the local CPU address bus line 1.
75,76	DLY1,DLY2	Delay 1 and delay 2. These delayed signals are used with DLY 0 to generate memory control signals.
77-80	$\overline{RAS3}$-$\overline{RAS0}$	Row address strobe line 3 - row address strobe line 0. The signals select memory banks 3 through 0, respectively. In this computer, the first two 512K banks are on the system board.
81	DLYOUT	Delay 0, 1, and 2 output enable. When this line is active, the delay line is enabled to generate memory control signals.
82	A2	Address line 2. This the local CPU address bus line 2.
83	PROCCLK	Processor clock. This signal is generated by the 82C211 bus controller.
84	VCC	+5 VDC.

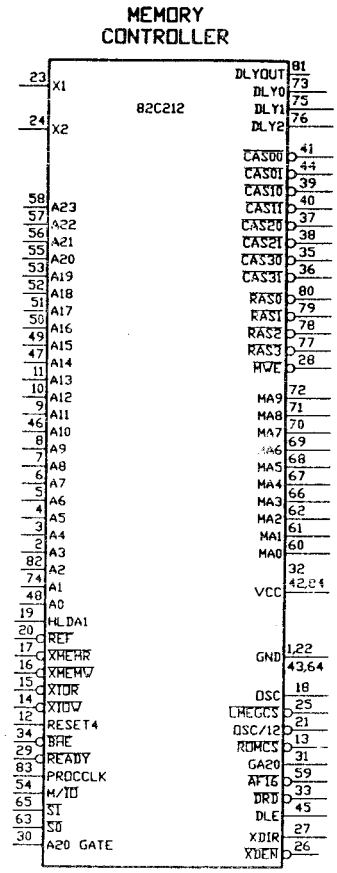


Figure 5-8. 82C212 Memory Controller Pinout

The Monitor ROM

Memory for the Monitor program is at FF1000H - FFFFFFH and requires 15 lines to address it. Since the Monitor ROM is read-only memory, no write signals reach it. The 82C212 memory controller generates $\overline{ROMCS}$, the ROM chip select signal. The 82C215 bus controller takes the data read from the ROM and passes it back to the data bus.

User Memory

Four banks of dynamic MOS 256-kilobit x 4 bit RAM ICs are used for the 1M of base memory. Table 5-8 describes the pin functions and Figure 5-9 shows the pinout for these devices.

Table 5-8. Base Memory RAM Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1-2	MDx	Memory data output.
3	$\overline{WE}$	Active-low write enable.
4	$\overline{RAS}$	Row address strobe.
5-8	NC	Not connected.
9-12	MA0-MA3	Memory address bits 0 through 3.
13	VCC	+5 VDC.
14-18	MA4-MA8	Memory address bits 4 through 8.
19-21	NC	Not connected.
22-23	#CAS#	Column address strobe.
24-25	MDx	Memory data output.
26	GND	Ground.

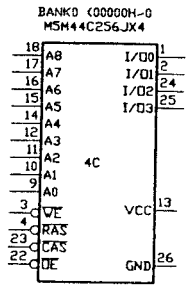


Figure 5-9. Base Memory RAM Pinout

Video Section

The video circuit is fed by the address bus, the data bus, and a number of control signals generated by the processor and support circuits. The address bus selects locations in video memory. Because the controller supports both static and dynamic memory devices, no external refresh circuits need to be provided.

Video controller — The V6366 controller is a 100-pin device that provides the address, data, and drive signals for displaying a video signal on either an LCD device or a CRT device. It retains the programmability and flexibility of the 6845 CRTC, which is the standard device used in PC-compatible color graphics (CGA) CRT applications, and adds features required for LCD applications.

Video memory — While the V6366 can support either static or dynamic memory devices, this computer uses static dynamic RAM. The video memory is 16K in two 8-kilobit x 8 devices. The base memory address is B8000H, standard for CGA video memory.

Character generator — The character generator is a programmed ROM that produces character patterns that are sent in parallel form to the parallel-to-serial shift register for conversion to a serial dot pattern.

External CRT — The external CRT that is supported by this computer should accept RGB and I (intensity) signals and have a horizontal resolution of 640 bits. Vertical resolution should be at least 200 lines.

V6366 Video Controller

The V6366 is a LCD and CRT controller that provides the signals necessary to produce video on the built-in LCD and composite monochrome and RGB/intensity video signals for use with external raster-scan CRT video monitors. New and expanded registers in the V6366 provide expanded color capabilities and LCD/CRT options that are not available in CGA designs. Full CGA and 6845 compatibility is maintained by the V6366 and support circuits. All video software that runs on CGA systems will run without need for modification on this computer. However, software

that is written to take advantage of the V6366's unique capabilities will not necessarily perform as expected on CGA systems.

The control section handles decoding of the control signals and communication between the internal registers and the system data bus. The CGA/CRT-LCD support circuits process the video memory data with information from the internal registers to produce the CRT and LCD video signals. The sync generator uses register information to produce the separate sync signals and combine them for the composite monochrome signal.

The V6366 video controller is a surface mounted, 100-pin, large-scale integrated circuit. The pins are described in Table 5-9 and illustrated in Figure 5-10.

Table 5-9. V6366 Video Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	$\overline{XA}$	This output signal is used to enable the video address buffers.
2	WE	Write enable. This output pin enables writing to the video RAM.
3	NC	Not connected.
4	$\overline{OE}$	Output enable. This is the output control for the video RAM.
5-12	LD7-LD0	LCD data bit 7 - LCD data bit 0. During LCD operation, these are the data bits sent to the LCD drivers. During CRT operation, LD7 - LD4 supply the red, green, blue, and intensity signals for the external monitor.
13	CSY	Composite sync.
14	BST	Color burst.
15	NC	Not connected.
16	$\overline{BLA}$	Blank.

Table 5-9 (continued). V6366 Video Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
17	HSY	Horizontal sync. This is the horizontal sync signal used for CRT operation.
18	VSY	Vertical sync. This is the vertical sync signal used for CRT operation.
19	$\overline{ESY}$	Not connected.
20-24	RD8-RD12	Video memory data line 8 - Video memory data line 12. These are the video memory data bus lines 8 through 12.
25	NC	Not connected.
26-29	RD13-RD15	Video memory data line 13 - video memory data line 15. These are the video memory data bus lines 13 through 15.
30	$\overline{LSW}$	Light pen switch. This pin is tied high. It is not used in this computer.
31	NC	Not connected.
32	$\overline{LDT}$	Light pen detection. This pin is tied high. It is not used in this computer.
33	RESET	Reset. This input signal clears all internal registers of the V6366. It is generated by the 82C211 bus controller as RESET4.
34-35	RD0-RD1	Video memory data line 8 - video memory data line 12. These are the video memory data bus lines 8 through 12.
36	NC	Not connected.

Table 5-9 (continued). V6366 Video Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
37-39	RD2-RD4	Video memory data line 8 - video memory data line 12. These are the video memory data bus lines 8 through 12.
40	VCC	+5 VDC.
41-43	RD5-RD7	Video memory data line 8 - video memory data line 12. These are the video memory data bus lines 8 through 12.
44	GND	Ground.
45	NC	Not connected.
46-48	A0-A2	Address line 0 - address line 2. These are the X address bus lines 0 through 2.
49	NC	Not connected.
50	A3	Address line 3. This is the X address bus line 3.
51	IOR	Input/output read. This is the active-low read signal for reading the contents of the I/O registers of the V6366.
52	IOW	Input/output write. This is the active-low write signal for writing to the I/O registers in the V6366.
53	NC	Not connected.
54	$\overline{\text{IOSEL}}$	Input/output select. This input pin is used as the chip select line for the V6366.
55-60	CD7-CD2	CPU data bit 7 - CPU data bit 2. These are the buffered CPU data bits from the SD data bus.
61	NC	Not connected.

Table 5-9 (continued). V6366 Video Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
62-63	CD1-CD0	CPU data bit 1 - CPU data bit 0. These are the buffered CPU data bits from the SD data bus.
64	BDIR	Not connected.
65	NC	Not connected.
66-70	RA0-RA4	Row address 0 - row address 4. These signals are used to address the Y matrix of the character generator.
71	MEMRDY	Memory ready. This is the video memory ready signal, indicating that video memory can be read from or written to. When low, video memory is busy.
72	MEMR	Memory read. This input pin controls reading from video memory.
73	MEMW	Memory write. This input pin controls writing to video memory.
74-76	AD15-AD13	Video memory address bit 15 - video memory address bit 13. These signals can be generated either by the V6366 or through the address buffers.
77	NC	Not connected.
78-80	AD12-AD10	Video memory address bit 12 - video memory address bit 10. These signals can be generated either by the V6366 or through the address buffers.
81	NC	Not connected.
82-85	AD9-AD6	Video memory address bit 9 - video memory address bit 6. These signals can be generated either by the V6366 or through the address buffers.

Table 5-9 (continued). V6366 Video Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
86	NC	Not connected.
87-89	AD5-AD3	Video memory address bit 5 - video memory address bit 3. These signals can be generated either by the V6366 or through the address buffers.
90	VCC	+5VDC
91-93	AD2-AD0	Video memory address bit 2 - video memory address bit 0. These signals can be generated either by the V6366 or through the address buffers.
94	GND	Ground.
95	NC	Not connected.

Table 5-9 (continued). V6366 Video Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
96	X1	Clock 1. This input pin receives the OSC clock signal from the 82C212 memory controller.
97	X2	Clock 2. This input pin receives the clock signal from the 18MHz crystal oscillator.
98	$\overline{EC}$	This output signal is used to control transmission of character font data on the RD bus.
99	NC	Not connected.
100	CCL	Video memory latch clock. This signal gates the signals from the video memory and latches them for the character generator.

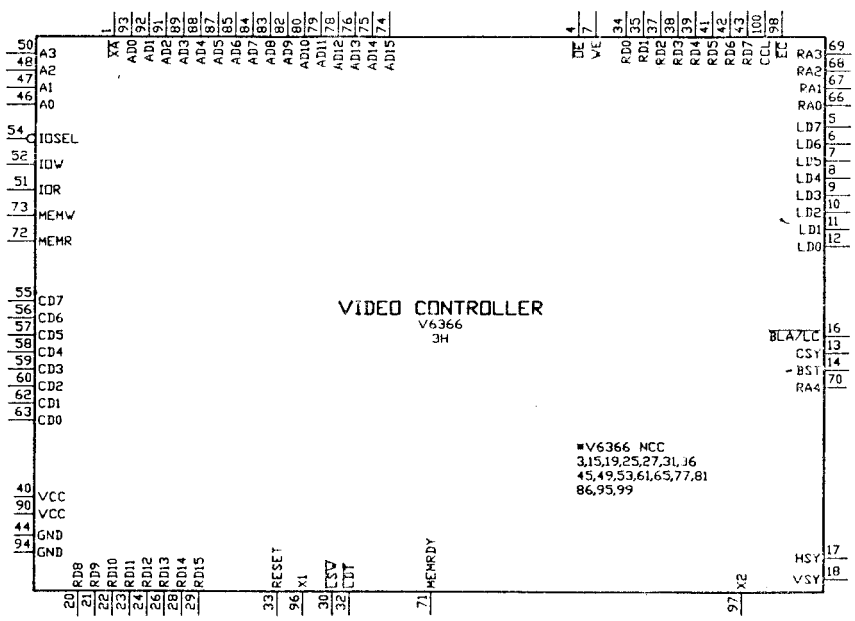


Figure 5-10. V6366 Video Controller Pinout

RGB Output Circuits

RGB output requires four digital signals: red, green, blue, and intensity. Intensity allows the computer to create an additional eight colors from the normal RGB output. The video controller places the R, G, B, and I signals on the LD4 - LD7 lines. It also places the horizontal sync signal on the HSY line and the vertical sync on the VSY line.

LCD/$\overline{\text{RGB}}$ is the control signal for RGB and LCD output. When the computer is in the RGB mode, LCD/$\overline{\text{RGB}}$ is low. When the computer is in the LCD mode, the opposite is true.

5J is an octal 3-state buffer. When LCD/$\overline{\text{RGB}}$ is low, 5J allows the signals on LD4 - LD7 to be passed through the buffer as R, G, B, and I signals, which go to pins 3, 4, 5, and 6 of connector CN2. When LCD/$\overline{\text{RGB}}$ is high, the outputs of the buffer float, resulting in no output, either high or low. The inductors help reduce RFI on the output.

The horizontal and vertical sync signals go through 5K, which ANDs those signals with $\overline{\text{LCD}}$/RGB. As long as the computer is the RGB mode, $\overline{\text{LCD}}$/RGB will be high, allowing the sync signals through the AND gates. During the LCD mode, $\overline{\text{LCD}}$/RGB is low, blocking the output of the AND gates (they are held low). The sync signals go to the connector through CL5 and CL6, which reduce the RF content of the signals. Refer to Figure 5-11 for a schematic of the RGB output circuits.

LCD Output Circuits

When the computer goes into the LCD mode, $\overline{\text{LCD}}$/RGB goes low, enabling the output of the LCD buffers in 5J and 6K. At the same time, LCD/$\overline{\text{RGB}}$ goes high and disables the RGB buffers.

The outputs of the video controller carry the signals that go to the buffers. These are passed through to connector CN6 on the main board. Capacitors reduce any ringing that can develop on the relatively long lines to the LCD driver board. Refer to Figure 5-12 for a schematic of the LCD output circuits.

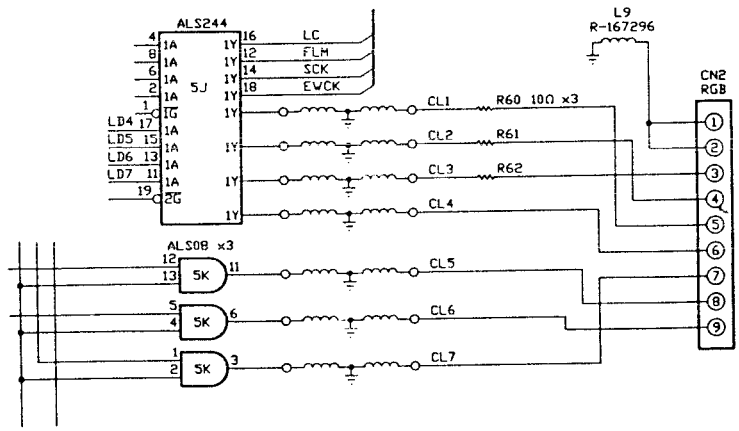


Figure 5-11. RGB Output

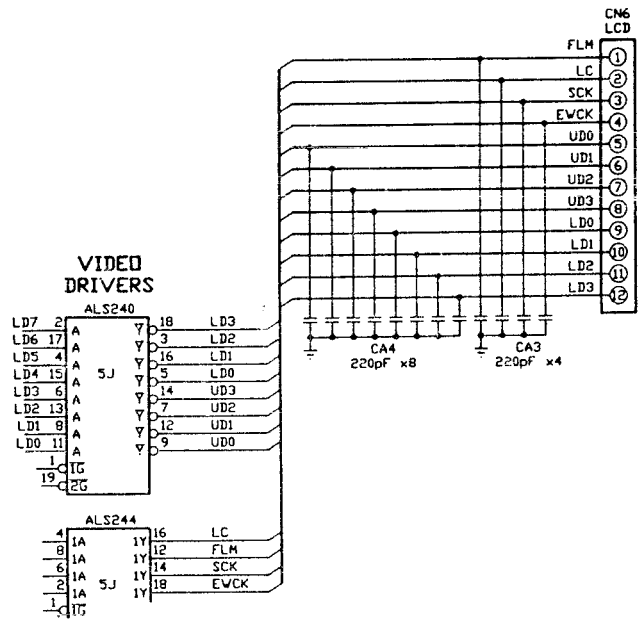


Figure 5-12. LCD Output

Parallel and Serial Communications Section

The SupersPort 286 Computer is supplied with one serial port and one parallel port. The circuits that control both the serial parallel ports consist of an 82C605 Multifunction Controller and various buffers and drivers that act as receivers and transmitters. Data transceivers handle the data bus interface.

The 82C605 Multifunction Controller

The 82C605 Multifunction Controller incorporates two UARTs, one parallel port, and one game port decoder. The UARTs are fully compatible with the NS16450 Asynchronous Communications Element. The parallel port contains the necessary control signals for use as a Centronics-compatible (output only) port. The pin functions of the 82C605 Multifunction Controller are described in Table 5-10 and the pinout is shown in Figure 5-13.

Note: Some units may have an 82C604 or 82C606 depending on which level of main circuit board is installed.

Table 5-10. 82C605 Multifunction Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	RESET	System reset.
2	GND	Ground.
3	NC	Not connected.
4	$\overline{\text{STBY}}$	Standby mode. Active when the main power supply is removed. It indicates that the bus interface is invalid and that no response should be made to any bus signals. This signal immediately terminates any bus signals in progress.
5	$\overline{\text{XENB}}$	External data bus enable. Internally ORed with the with the signal used to generate the $\overline{\text{DBENB}}$ output.
6	$\overline{\text{DBENB}}$	Data bus driver enable. Used to enable data buffer U6H.

Table 5-10 (continued) 82C605 Multifunction Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
7	$\overline{\text{DBIN}}$	Data bus driver direction. Used to control the direction of U6H.
8	$\overline{\text{RTS2}}$	Request to send. Not connected.
9	VCC	+5 VDC.
10	X1	1.8432 MHz clock signal input used by the internal UARTs.
11	X2	Output for the clock signal used by the UARTS.
12	$\overline{\text{DTR2}}$	Data terminal ready. Not connected.
13	$\overline{\text{CTS2}}$	Clear to send. Not connected.
14	$\overline{\text{DSR2}}$	Data set ready. Not connected.
15	$\overline{\text{DCD2}}$	Data carrier detect. Not connected.
16	$\overline{\text{RI2}}$	Ring indicator. Not connected.
17	RXD2	Not connected.
18	TXD2	Not connected.
19	$\overline{\text{RTS1}}$	Request to send. Handshake signal which notifies a MODEM or data set that UART 1 is ready to transmit data.
20	$\overline{\text{DTR1}}$	Data terminal ready. Notifies the MODEM or data set that UART 1 is ready to transfer characters.
21	$\overline{\text{CTS1}}$	Clear to send. Handshake signal which notifies UART 1 that a MODEM is ready to receive data.
22	$\overline{\text{DSR1}}$	Data set ready. Handshake signal for UART 1. Tells the CPU that the MODEM or data set is ready to transmit characters.

Table 5-10 (continued) 82C605 Multifunction Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
23	$\overline{\text{DCD1}}$	Data carrier detect. Notifies UART 1 that a carrier signal has been detected by a MODEM.
24	$\overline{\text{RI1}}$	Ring indicator. Notifies UART 1 that a telephone ringing signal has been detected by a MODEM or data set.
25	RXD1	Input pin for the serial data stream to UART 1.
26	TXD1	Output pin for the serial data stream to UART 1.
27	GND	Ground.
28	IRQ7	Interrupt request 7. This signal is used for parallel port 1.
29	IRQ5	Interrupt request 5. This signal is used for parallel port 2.
30	IRQ4	Interrupt request 4. This signal is used for UART 1 (COM 1).
31	IRQ3	Interrupt request 3. This signal is used for UART 2 (COM 2).
32	$\overline{\text{IOW}}$	I/O write strobe.
33	AEN	Address enable. Used to gate $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$.
34	$\overline{\text{IOR}}$	I/O read strobe.
35	ERROR	Error. Indicates printer error.
36,37	SA9, SA8	Two high order bits of the address bus.
38	ACK	Acknowledge. Printer handshake signal indicating data has been received.
39	$\overline{\text{BUSY}}$	Busy signal. Indicates the printer is unable to receive data.

Table 5-10 (continued) 82C605 Multifunction Controller Pin Descriptions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
40	$\overline{PE}$	Paper end signal. Indicates the printer is out of paper.
41	$\overline{SLCT}$	Select. Indicates the printer is selected.
42	SELECT	Unit select. This pin is connected to SAD0 - SAD7 and is used to identify a particular circuit.
43	VCC	+5 VDC.
44-51	SAD7-SAD0	Multiplexed address/data bus.
52	ALE	Address latch enable.
53	$\overline{ABENB}$	Address buffer/multiplex enable. Used to enable address buffer U7H.
54-60,62	PD7-PD0	Parallel port data bus. This is the output from the printer.
61	GND	Ground.
63	SLCTIN	Select in. This signal selects the printer.
64	INIT	Initialize. This initializes the printer.
65	AUTOFD	Auto feed. Causes the printer to generate a line feed after each line is printed.
66	STROBE	Strobe. This is the printer data strobe.
67	$\overline{GAME}$	Game port enable. Not connected.
68	$\overline{PS}$	Power sense. Not connected.

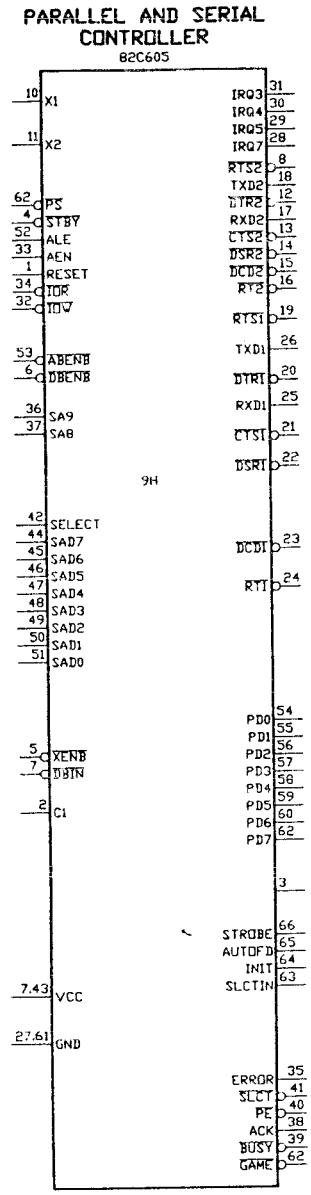


Figure 5-13. 82C605 Multifunction Controller Pinout

Mass Storage Section

Only one floppy disk drive may be installed in this computer. The operating system and the devices used in this computer will support high-density 3.5-inch floppy disk drives, dual-speed high-density 5.25-inch floppy disk drives (externally), and standard-density 5.25-inch floppy disk drives (externally). One 3.5-inch, half-height, 20M or 40M hard disk drive is also installed.

37C65A Floppy Disk Controller

The disk controller provides an interface between the CPU and the disk drives. When reading a disk, the controller converts the serial data from the disk drive to parallel data. When writing to a disk, the controller converts the parallel data to a serial form that can be written to the disk. The controller also adds a number of timing signals before sending the data to the selected drive.

The 37C65A disk controller in this computer is an extended CMOS version of the 765 disk controller used in most PC-compatible designs. The 37C65A can also handle the format required to read from and write to 3.5-inch disks. This device contains control functions to interface the CPU and up to four disk drives. It supports FM and MFM disk encoding formats and can be operated in DMA and non-DMA modes.

The 37C65A FDC requires a +5 VDC voltage for normal operation. The clock signal used for this device is a single phase 8 MHz square wave. The pinout for this device is illustrated in Figure 5-14. Table 5-11 describes the signals used by the 3765 FDC.

Table 5-11. 37C65A Floppy Disk Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	$\overline{RD}$	Read. A low on this input allows data transfers from the FDC to the bus. A high on the $\overline{CS}$ line disables this input.
2	$\overline{WR}$	Write. A low on this input allows data transfers from the bus to the FDC. A high on the $\overline{CS}$ line disables this input.
3	$\overline{CS}$	Chip select. This active-low input selects the FDC and enables $\overline{RD}$, $\overline{WR}$, and A0.
4	A0	Data/status register selection. A high on this input selects the data register contents and a low selects the status register contents for transfer to the data bus.
5	$\overline{DACK}$	DMA acknowledge. This input line is held low during an active DMA cycle, while the FDC is performing a DMA transfer.
6	TC	Terminal count. This output line indicates DMA cycle completion when high. It also terminates data transfers during read, write, and scan commands in either DMA or non-DMA mode.
7 - 14	D0 - D7	8-bit bidirectional data bus. These lines are disabled when $\overline{BCS}$ is held high.
15	DMA Data	DMA request. The FDC requests a DMA transfer by asserting this output (DRQ = 1).
16	IRQ	Interrupt. This output is the FDC interrupt request line.
17	$\overline{DCHNG}$	Connected to ground.
18	$\overline{LDOR}$	Load operations register. Address decode which enables the loading of the operations register. Internally gated with $\overline{WR}$ to create the strobe that latches the data bus into the operations register.

Table 5-11 (continued). 37C65A Floppy Disk Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
19	$\overline{\text{LDCR}}$	Load control register. Address control which enables the loading of the control register. Internally gated with $\overline{\text{WR}}$ to create the strobe that latches the two LSB's from the data bus into the control register.
20	RESET	Reset. This input resets the output lines and places the FDC in an idle state. If the RDY input is held high during RESET, an interrupt will be generated within 1.024 ms. To clear the interrupt, use the sense interrupt status command.
21	RDD	Read data. This is the serial data and clock input line used for reading data from the drive.
22	$\overline{\text{XT2}}$	Crystal oscillator drive output.
23	XT2	Crystal oscillator drive input used for non-standard data rates.
24	DRV	Drive type. Set at logic 1 for use with single speed drive motors.
25	$\overline{\text{XT1}}$	Crystal oscillator drive output.
26	XT1	Crystal oscillator input. This requires a 16 MHz crystal and is used for all standard data rates.
27	PCVAL	Precompensation value. These outputs reflect the write precompensation status for MFM mode. They indicate early, late, or normal timing; set for 125 ns.
28	$\overline{\text{HS}}$	Head select. This output line reflects the head selected: logic 1 = side 0, logic 0 = side 1.

Table 5-11 (continued). 37C65A Floppy Disk Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
29	$\overline{\text{WE}}$	Write enable. This output line enables writing data to disk.
30	$\overline{\text{WD}}$	Write data. This serial clock and data output line transfers data to disk.
31	$\overline{\text{DIRC}}$	Direction. This output determines the direction of the head stepper motor: logic 1 = outward motion, logic 0 = inward motion.
32	$\overline{\text{STEP}}$	Step pulse. This line issues a pulse for every track-to-track movement.
33	$\overline{\text{DS1}}$	Drive select 1. This signal originates in the operations register and enables the interface in disk drive number 1.
34	GND	Ground.
35	$\overline{\text{DS2}}$	Drive select 2. This signal originates in the operations register and enables the interface in disk drive number 2.
36	$\overline{\text{MO1}}$,$\overline{\text{DS3}}$	Motor on 1, drive select 3. In PC/AT mode, this signal enables the MOTOR ON signal for disk drive number 1. In base or special mode, this signal enables disk drive number 3.
37	$\overline{\text{MO2}}$, $\overline{\text{DS4}}$	Motor on 2, drive select 4. In PC/AT mode, this signal enables the MOTOR ON signal for disk drive number 2. In base or special mode, this signal enables disk drive number 4.
38	$\overline{\text{HDL}}$	Head load. This output line causes the read/write heads to contact the disk.

Table 5-11 (continued). 37C65A Floppy Disk Controller Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
39	$\overline{RWC}$,$\overline{RPM}$	Reduced write current, revolutions per minute. This output causes a reduced write current when bit density is increased toward the inner tracks, becoming active with numbers 29 and larger. In the PC/AT mode, this signal will be active when the 250 MFM or 125 FM data rate is selected.
40	DCHNG	Disk change. This signal is active when a high density drive is attempting to format a low density diskette.
41	$\overline{WP}$	Write protected. This input senses write protection on a disk.
42	$\overline{TR00}$	Track 00. This input senses when the head is positioned over the outermost track.
43	$\overline{IDX}$	Index. A high on this input indicates the beginning of a disk track.
44	Vcc	+5 VDC power.

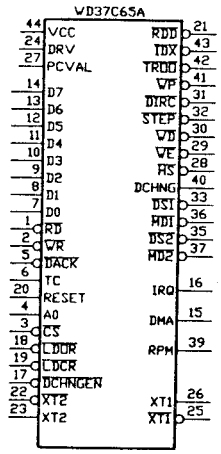


Figure 5-14. 37C65A Floppy Disk Controller Pinout

Keyboard

The keyboard in this computer is strobe-scanned and controlled by a keyboard processor. The keyboard circuits are contained on two boards: the main board, which contains the keyboard controller; and the keyboard itself, which contains the keyswitch matrix.

Keyboard controller — The keyboard controller is a dedicated microprocessor that contains 4K of preprogrammed ROM and 128 bytes of RAM. The controller strobe-scans the keyboard and is programmed to handle N-key rollover.

Keyswitch matrix — The 79 keys of the keyboard are configured in a matrix consisting of 10 scan lines and 8 read lines. Each keyswitch is placed in the matrix with a diode to prevent false scan codes from being generated when more than one key is pressed.

Power Supply

The power supply provides the voltages used by the various circuits in the computer. Power for the supply comes from an external adapter (120-volt AC line, 240-volt AC line, or 12-volt DC cigarette lighter) or an internal battery.

Input power — The AC adapters provide approximately +18 volts of regulated DC. The DC cigarette lighter adapter supplies unchanged DC power from an automotive-type 12-volt system. The battery also provides a DC voltage through the input power circuits. These circuits provide three functions: internal battery power, external adapter power, and a charging circuit. The battery is protected from overcharging by internal power supply regulation.

Output power — The computer requires a regulated +5 VDC to operate. RS-232C operation requires a regulated -5 VDC. The power supply also provides a regulated +12 VDC for the disk drive circuits. These supplies are developed from the DC input voltage, which can vary from slightly under +12 VDC with the system running from the battery to as much as +21 VDC with an AC adapter and a fully-charged battery.

NOTE: In systems using a hard disk drive, the power levels are monitored by the low voltage detection circuits. If the voltage drops below a pre-determined point, it will not be possible to access the hard disk drive. If this happens you must connect an external adapter to the computer and recharge the battery.

Backlight power — The backlight power is the only AC output of the power supply. The backlight requires an AC signal of about 750 Hz with a voltage range from about 20 VAC (low backlight) to about 80 VAC (bright backlight). The backlight circuit consists of three parts: the drive, which includes the brightness control; the on/off control, which is controlled by the ELON signal from the computer; and the oscillator, which produces the output to the backlight. The ELG circuit shuts the backlight off when the contrast control is slid to the minimum position.

Chapter 6

Troubleshooting

This chapter provides a troubleshooting procedure intended to isolate hardware faults to circuit board level only. The SupersPort 286 portable computer is not supported to the component level.

Troubleshooting Procedure

The troubleshooting procedure is in a question-and-answer form, with a yes or no answer for most questions. You will be directed to the next step by the YES or NO column. If a "—" is shown in either or both columns:

- The fault has been identified and corrected. In this case the step directs you to retest the fault area to verify that the problem has been corrected.
- Further action is required. In this case the step directs you to perform a specific test to isolate the problem.

The steps contained in this procedure are:

Step 1: Initial Checks
Step 2: Power Up
Step 3: ROM-Based Disk Read Test
Step 4: Disk-Based Diagnostics Fast Tests
Step 5: Comprehensive ROM-Based Tests
Step 6: Comprehensive Disk-Based Diagnostics
Step 7: Power Supply
Step 8: Main Board
Step 9: Floppy Disk Drives
Step 10: Hard Disk Drives
Step 11: Liquid Crystal Display
Step 12: Keyboard

Configuring the disk-based diagnostics is covered at the end of this chapter.

Step 1: Initial Checks

STEP	PROCEDURE	YES	NO
1	Is the computer plugged into a working external adapter, and is the adapter plugged into a working outlet?	1a	2
1a	Perform a "sense test" of the computer. Check for damage to the cabinet, disk drives, keyboard, and LCD. Check the floppy disk drive for a jammed disk in the drive and improper mechanical operation. Also, smell the computer for indications of overheated or burned components. Do you detect any possible damage?	1b	2
1b	Locate and replace damaged parts or free any jammed disk. Proceed to step 2.	—	—

Step 2: Power Up

STEP	PROCEDURE	YES	NO
2	Plug the computer into a working external adapter. Turn on the computer. You should see the LCD light up. After a few seconds you should hear the disk drive start and see the drive active LED light. Do you hear, see, or smell anything unusual?	2a	2b
2a	Turn the computer off and return to step 1a	—	—

STEP	PROCEDURE	YES	NO
2b	Did the computer power up?	2d	2c
2c	Turn off the computer. Proceed to step 7.	—	—
2d	Is there a readable display on the LCD?	3	2e
2e	Turn off the computer. Proceed to step 11	—	—

Step 3: ROM-Based Disk Read Test

STEP	PROCEDURE	YES	NO

3	Defeat autoboot by turning the computer off for at least 30 seconds and then turning it back on and pressing the CTRL-ALT-INS key combination. After defeating autoboot, the Monitor program prompt should appear in the upper left corner of the screen:
	
	`MFM-200 Monitor, Version x.x`
	`Memory Size: xxxK bytes`
	`Enter "?" for help.`
	`->_`
	
	Does this message appear?
		3c	3a

3a	Reset the computer by pressing the CTRL-ALT-INS key combination. After resetting the computer, the Monitor program prompt should appear in the upper left corner of the screen:
	
	`MFM-200 Monitor, Version x.x`
	`Memory Size: xxxK bytes`
	`Enter "?" for help.`
	`->_`
	
	Does this message appear?
		3c	3b

3b	Turn off the computer and proceed to step 8.	—	—
3c	Type TEST and press the ENTER key. Does the test menu appear on the screen?	3d	3b
3d	Insert a disk in drive A (be sure you have a backup copy of this disk). Can the disk be inserted and does it latch in place?	3f	3e
3e	Turn the computer off and proceed to step 9.	—	—

3f	Select the disk read test from the menu by pressing the 1 key. The message:
	
	`DISK READ TEST`
	`TEST COUNT = x`
	`TYPE <ESC> TO ABORT`
	
	should appear on the screen. Allow the disk read test to run for at least 30 seconds. Does a device error message appear on the screen?
		3g	4

3g	Turn off the computer and proceed to step 9.	—	—

Step 4: Disk-Based Diagnostics Fast Tests

STEP	PROCEDURE	YES	NO
4	Insert the disk-based diagnostics disk into drive A and boot the drive. Does the diagnostics menu appear on the screen?	4d	4a
4a	Insert another bootable disk into drive A and boot the drive. Can you boot the drive?	4b	4c
4b	Use another copy of the disk-based diagnostics and return to step 4.	—	—

STEP	PROCEDURE	YES	NO
4c	Proceed to step 9.	—	—
4d	Using the arrow keys, select the diagnostics for the computer you are servicing. If that computer model does not appear on the menu, proceed to "Configuring the Disk-Based Diagnostics" at the end of this chapter. Run the fast test. Does an error or fail message appear on the screen?	4e	5
4e	Run all the automatic tests for the device that showed an error in the fast tests. Does an error or fail message appear on the screen?	4f	5
4f	Refer to Table 6-1 and proceed to the appropriate step to repair or replace the faulty device.	—	—

Table 6-1. Error Messages

ERROR MESSAGE	STEP
CPU failure!	8
ROM checksum failure!	8
RAM failure! Address: xxxx:yyyy, Bit: N, Chip: Uxxx	8
Parity hardware failure! Address: xxxx:yyyy, Bit: N,Chip: Uxxx	8
Parity failure! Address: xxxx:yyyy, Bit: N, Chip: Uxxx	8
Timer Interrupt failure!	8
Invalid/No keyboard code received!	13
Drive not ready!	9
No System	9
Bad disk controller!	9
DMA overrun error!	8
Sector not found!	9
CRC error!	9
Invalid address mark detected!	9
Seek Failure!	9
DEVICE ERROR	9

Step 5: Comprehensive ROM-based Tests

STEP	PROCEDURE	YES	NO
5	Does the computer have more than one drive?	5a	5c
5a	Boot the additional drives and run the ROM-based disk read test on each drive. Does an error or fail message appear on the screen?	5b	5c
5b	Proceed to step 9 (floppy disk drives) or step 10 (hard disk drives).	—	—
5c	Run the ROM-based memory test. Allow the test to run for at least two passes. Does an error or fail message appear on the screen?	5d	5e
5d	Proceed to step 8.	—	—
5e	Run the ROM-based keyboard test (refer to Table 6-3 later in this chapter). Is the information displayed on the screen correct for each key?	5f	5g
5f	Do any error or fail messages appear on the screen?	5g	5h
5g	Proceed to step 12.	—	—
5h	Run ROM-based power-up test. Allow the test to run for at least ten passes. Do any error or fail messages appear on the screen?	5i	6
5i	Refer to Table 6-1 and proceed to the appropriate step to repair or replace the faulty device.	—	—

Step 6: Comprehensive Disk-Based Diagnostics

STEP	PROCEDURE	YES	NO
6	Select the normal tests for the computer from the disk-based diagnostics menu. (enter NO when prompted for fast tests). Run all of the automatic tests for the computer. Do any error or fail messages appear on the screen?	6a	6b
6a	Refer to Table 6-1 and proceed to the appropriate step to repair or replace the faulty device.	—	—
6b	Run all manual tests by selecting each test individually (select SINGLE TEST) and running sections marked M (manual) or C (combination). Does an error or fail message appear on the screen?	6a	7

Step 7: Power Supply

STEP	PROCEDURE	YES	NO
7	Is the computer plugged into an operating external adapter and electrical outlet?	7b	7a
7a	Plug the computer into an operating electrical outlet. Return to step 2.	—	—
7b	Turn on the power switch. Does the computer power up?	2d	7c
7c	Check the output voltage of the external adapter. Is the output voltage at least +16 VDC?	7e	7d
7d	Replace the external adapter and return to step 7.	—	—

STEP	PROCEDURE	YES	NO
7e	Refer to Chapter 3 and separate the display from the base unit. Remove connectors CN305 and CN306 from the power supply assembly. With the external adapter plugged into the computer, turn on the power switch. Check the connector pins for the voltages shown in Table 6-2.		

Table 6-2. Power Supply Voltages

CONNECTOR NUMBER	PIN NUMBER	VOLTAGE
CN305	1	+12 VDC
	2	0 VDC
	3	0 VDC
	4	+5 VDC
CN306	1	+5 VDC
	2	0 VDC

	Are the indicated voltages present?	7f	7g
7f	Plug the connectors back in and proceed to step 8.	—	—
7g	Replace the power supply. Return to step 2 to verify the problem has been corrected.	—	—

Step 8: Main Board

STEP	PROCEDURE	YES	NO
8	Verify that the computer is plugged into a working outlet and turn the computer on. Does the computer power up?	8b	8a

STEP	PROCEDURE	YES	NO
8a	Perform the checks listed under step 7. If you reach this step without locating the problem, replace the main board. Return to step 2 to verify the problem has been corrected.	—	—

8b	Press the CTRL-ALT-INS key combination. The Monitor program prompt should appear in the upper left corner of the screen:
	`MFM-200 Monitor, Version x.x`
	`Memory Size: xxxK bytes Enter "?" for help. ->_`
	Does the correct message appear?
		3c	8c

8c	Place the MS-DOS Distribution Disk in drive A and type B0 followed by the ENTER key. Except for the display, did the computer operate normally and boot the disk?	11	8d
8d	Turn the computer off and separate the display from the base unit (refer to Chapter 3). Perform a sense test (see step 1a). Do you detect any damage?	8e	8f
8e	Replace any assemblies that are damaged and return to step 2 to verify that the problem has been corrected.	—	—
8f	Check the wire and cable connectors. Are all the connectors properly seated?	8h	8g
8g	Properly seat all connectors and repeat step 8. Does the correct message appear?	3c	8h
8h	Replace the keyboard (refer to Chapter 3) and repeat step 8. Is the display correct?	3c	8i
8i	Refer to Chapter 4. Are the jumpers set correctly?	8k	8j
8j	Correct the jumper settings and return to step 2 to verify that the problem has been corrected.	—	—
8k	Replace the main board. Return to step 2 to verify that the problem has been corrected.	—	—

Step 9: Floppy Disk Drives

STEP	PROCEDURE	YES	NO
9	Be sure you have a backup copy of the disk used in these steps. Can a floppy disk be inserted into drive A?	9	9a
9a	Visually inspect the drive for mechanical problems. Is there a disk in the drive?	9b	9c
9b	Attempt to remove the disk by pressing the disk eject button. Can the disk be removed from the drive?	9e	9c
9c	Carefully grasp the disk with a pair of tweezers and gently remove it from the drive. If the disk will not move or the tweezers slip off, the disk is jammed. Is the disk jammed?	9d	9e
9d	Separate the display from the base unit and replace the drive (refer to Chapter 3). Return to step 2 to verify that the problem has been corrected.	—	—
9e	Insert a disk into the drive. Does the disk latch into place?	9f	9d
9f	Press the eject button. Did the disk eject?	9g	9d

STEP	PROCEDURE	YES	NO
9g	Remove the disk from the drive and inspect it for damage. Is the disk damaged?	9d	9h
9h	Turn the computer on and defeat the autoboot feature by pressing the CTRL-ALT-INS key combination. Proceed to step 9i.	—	—
9i	Insert a copy of the MS-DOS Distribution Disk in drive A. Boot the drive by typing B0 at the Monitor prompt and pressing the ENTER key. Does the disk access LED light?	9j	9k

9j	A message similar to the following should appear on the screen:
	`A>DATE`
	`Current date is Tue 1-01-1980`
	`Enter new date:_`
	Does the correct message appear?
		4	9k

9k	Remove the disk from the drive and turn the computer off. Remove the access cover from the bottom of the computer and verify that the jumpers on the main board are properly set. Are all jumpers properly set?	9m	9l
9l	Properly set the jumpers and repeat step 9i. Does the correct message appear?	4	9m
9m	Separate the display from the base unit and check the wire and cable connectors. Are all the connectors properly seated?	9o	9n
9n	Properly seat all connectors and repeat step 9i. Does the correct message appear?	4	9o
9o	Check the drive select jumper on the disk drive. Is it set for drive 0?	9q	9p
9p	Correct the jumper setting and repeat step 9i. Does the correct message appear?	4	9q
9q	Replace the floppy drive control cable, which connects the main board to the floppy disk drives (refer to Chapter 3). Repeat step 9i. Does the correct message appear?	4	9r
9r	Replace drive A and repeat step 9i. Does the correct message appear?	4	9s
9s	Disconnect, but do not remove, drive A. Attempt to boot the hard disk drive by typing BW and pressing ENTER. Does the correct message appear?	9t	9u
9t	Reconnect drive A and disconnect, but do not remove, the hard disk controller card and hard disk drive from the computer. Repeat step 9i. Does the correct message appear?	10	9u
9u	Replace drive A (refer to Chapter 3). Repeat step 9i. Does the correct message appear?	4	9v
9v	Replace the main board. (refer to Chapter 3). Repeat step 9i. Does correct message appear?	9w	9k
9w	Proceed to step 10 to make sure the hard disk drive operates properly.	—	—

STEP	PROCEDURE	YES	NO

Step 10: Hard Disk Drive

Step 10: Hard Disk Drive

STEP	PROCEDURE	YES	NO
10	Visually inspect the hard disk drive. Do you see any damage?	10a	10b
10a	Replace or repair damaged parts and return to step 4 to verify that the problem has been corrected.	—	—
10b	Turn the computer on. Does the hard drive LED light?	10c	10
10c	Did the hard disk drive boot?	4	10e

10d	Attempt to boot the hard disk drive by pressing the CTRL-ALT-INS key combination. Type BW and press the ENTER key. A message similar to the following should appear on the screen:
	`Current date is Tue 1-01-1980`
	`Enter new date:_`
	Does the correct message appear on the screen?
		4	10e

10e	Does the message `No system` appear on the screen?	10f	10g
10f	Attempt to install MS-DOS on the hard disk by inserting a copy of the MS-DOS Distribution Disk in drive A and booting it. Type XCOPY A: C: /V and press ENTER. Repeat step 10d. Does the correct message appear?	4	10g
10g	Turn the computer off and separate the display from the base unit (refer to Chapter 3). Perform a sense test (see step 1a). Refer to Chapter 4 and verify that the jumpers are set properly. Do you detect any damage or improper configuration?	10h	10i
10h	Replace any damaged assemblies and properly set the jumpers. Return to step 4 to verify that the problem has been corrected.	—	—
10i	Check the wire and cable connectors. Are all the connectors properly seated?	10k	10j
10j	Properly seat all connectors. Repeat step 10d. Does the correct message appear?	4	10k
10k	Replace the ribbon cable that connects the hard disk drive to the hard disk drive controller card. Repeat step 10d. Does the correct message appear?	4	10l
10l	Replace the hard disk controller card (refer to Chapter 3). Repeat step 10d. Does the correct message appear?	4	10m
10m	Replace the main board (refer to Chapter 3). Repeat step 10d. Does the correct message appear?	4	10n
10n	Replace the hard disk drive (refer to Chapter 3). Run the PREP utility and return to step 10f to install MS-DOS on the new hard disk. Return to step 4 to make sure that the problem has been corrected.	—	—

Step 11: Liquid Crystal Display

STEP	PROCEDURE	YES	NO
11	Verify that the computer is plugged into a working outlet and turn the computer on. Does the computer power up?	11a	8

STEP	PROCEDURE	YES	NO

11a	Press the CTRL-ALT-INS key combination. The Monitor program prompt should appear in the upper left corner of the screen:
	
	`MFM-200 Monitor, Version x.x`
	`Memory Size: xxx`
	`K bytes Enter "?" for help.`
	`->_`
	
	Does the correct message appear?
		3c	11b

11b	Place the MS-DOS Distribution Disk in drive A and type B0 followed by the ENTER key. Except for the display, did the computer operate normally and boot the disk?	11c	8
11c	Turn the computer off and separate the display from the base unit (refer to Chapter 3). Perform a sense test (see Step 1a). Do you detect any damage?	11d	11e
11d	Replace any assemblies that are damaged and return to step 2 to verify that the problem has been corrected.	—	—
11e	Check the wire and cable connectors. Are all the connectors properly seated?	11g	11f
11f	Properly seat all connectors and repeat step 11. Does the correct message appear?	3c	11g
11g	Open the display (refer to Chapter 3) and perform a sense test (see step 1a). Do you detect any damage?	11h	11i
11h	Replace any assemblies that are damaged and return to step 2 to verify that the problem has been corrected.	—	—
11i	Perform a continuity check on the main LCD cable. Are there any open wires?	11j	11k
11j	Replace the LCD cable and return to step 2 to verify that the problem has been corrected.	—	—
11k	Replace the LCD assembly and repeat step 11. Does the correct message appear?	3c	11l
11l	Replace the main board. Return to step 2 to verify that the problem has been corrected.	—	—

Step 12: Keyboard

STEP	PROCEDURE	YES	NO
12	Inspect the keyboard. Do you see any damage?	12a	12b
12a	Replace the damaged keyboard (refer to Chapter 3). Proceed to step 12b.	—	—

12b	Turn the computer on and press the CTRL-ALT-INS key combination. The Monitor program prompt should appear in the upper left corner of the screen:
	
	`MFM-200 Monitor, Version x.x`
	`Memory Size: xxxK bytes Enter "?" for help. ->_`
	
	Does the correct message appear?
		12c	12j

12c	Type TEST at the Monitor prompt. If the word TEST is echoed accurately on the screen, press ENTER and proceed to step 12d If the word TEST is not echoed accurately on the screen, proceed to step 12h.	—	—

STEP	PROCEDURE	YES	NO
12d	Select the keyboard test by pressing the 2 key. The keyboard test identification and character code message should appear across the top of the screen. The message `Type <ESC> to exit` should appear in the bottom left corner of the screen. Does the correct display appear?	12e	12j
12e	Press each of the keys on the keyboard. The screen should fill with the character pressed and the message at the top of the screen should change to read: `KEYBOARD TEST  CHARACTER CODE = xxxxH` Does the correct character appear on the screen for each key pressed?	12f	12j
12f	Press the CAPS LOCK key on the keyboard. Does the CAPS LOCK LED light?	12g	12j
12g	Press the NUMLOCK key. Does the NUMLOCK LED light?	12h	12j
12h	Press FN-PDLOCK. Does the PADLOCK LED light?	12i	12j
12i	Press FN-SCROLL LOCK. Does the SCROLL LOCK LED light?	4	12j
12j	Turn the computer off. Separate the display from the base unit (refer to Chapter 3) and perform a sense test (see step 1a). Do you detect any damage?	12k	12l
12k	Replace any damaged assemblies. Turn the computer back on and repeat step 12b. Does the correct display appear?	12c	12l

STEP	PROCEDURE	YES	NO
12l	Check the wire and cable connectors. Are all the connectors properly seated?	12n	12m
12m	Properly seat all connectors. Turn the computer back on and repeat step 12b. Does the correct display appear on the screen?	12c	12n
12n	Replace the keyboard (refer to Chapter 3). Repeat step 12b. Does the correct display appear on the screen?	12c	12o
12o	Replace the main board (refer to Chapter 3). Repeat step 12b. Does the correct display appear on the screen?	12c	12l

Configuring the Disk-Based Diagnostics

Configuring the disk-based diagnostics usually requires adding the test for a hard disk drive. The procedure described in this section for adding a hard disk drive test can also be used to add other tests. Refer to the disk-based diagnostics manual for specific information about configuring other tests.

1. Select a Z-200 computer model from the diagnostics menu with the arrow keys. Press ENTER to enter the selection.

2. At the fast test prompt, enter NO. Use the arrow keys to move the cursor to the correct response. Press ENTER to enter the selection.

3. When the diagnostic test menu appears on the screen, use the arrow keys to select configuration. Press ENTER to enter the selection.

4. When the configuration test menu appears on the screen, use the arrow keys to select CONFIGUR TEST. Press ENTER to enter the selection.

5. The cursor moves up into the list of available

5. The cursor moves up into the list of available diagnostic tests. Using the arrow keys, select WINCHESTER-XT DIAGNOSTIC. Press ENTER to enter the selection.

6. The diagnostics read the hard disk drive type and other configuration data from the configuration switch. An improperly configured computer may cause the diagnostics to fail. Refer to Chapter 4 and verify the computer's configuration. When a (C) appears after the WINCHESTER-XT DIAGNOSTIC field, the cursor will move back to the CONFIGUR TEST field.

NOTE: You can use the DSKUTL.HLP utility to check the current configuration settings. This utility is on the diagnostic disk.

7. Use the arrow keys to select exit. Press ENTER to enter the selection.

8. At the prompt, use the arrow keys to indicate that you wish to write the configuration to the disk. Press ENTER to enter this selection.

9. At the prompt, type the model number (ZWL-200) and press ENTER to enter it.

10. Continue using the arrow keys to select exit and pressing ENTER to enter the selection until the model selection menu appears on the screen.

Chapter 7
Parts Lists

This chapter provides an exploded view of the ZWL-200-2 and ZWL-200-4 computers and a computer parts list.

Table 7-1. ZWL-200-2 and ZWL-200-4 Exploded Parts List

REFERENCE NUMBER	ZDS PART NUMBER	DESCRIPTION
1	89-0065	AC power cord
2	100-1919	Battery pack
3	150-0308	AC adapter
4	150-0382	Housing and charging PCB
5	150-0383	Battery
6	969-0954	Cabinet, LCD front
7	969-0876	Cover, power switch
8	969-0877	Cover, modem
9	969-0878	Cover, configuration selection access
11	969-0879	Blank panel, hard drive
12	969-0880	Latch assembly, left
13	969-0881	Latch assembly, right
14	969-0882	Hinge cover assembly, left
15	969-0883	Hinge cover assembly, right
16	969-0884	Hinge assembly, left
17	969-0885	Hinge assembly, right
18	969-1197	Floppy disk drive, 2 M, 3-1/2 inch
21	969-1198	Shield, floppy drive
22	969-1199	Cable, floppy drive power
23	969-0894	Cable, floppy drive controller
24	969-0896	Bracket, floppy drive
25	969-0957	LCD assembly, with back light
26	969-0961	Cable, main board to LCD
27	969-0969	Sheet, brightness/contrast
28	969-0968	Knob, brightness/contrast
31	969-1196	Power PCB assembly with switch
32*	969-0998	Power switch PCB assembly
33	969-0955	LED PCB assembly
34	969-1194	Keyboard assembly
35*	969-1195	Keyboard only
36	969-0911	Speaker assembly
37	969-0912	Handle
38	969-0913	Cover, LCD cable
39	969-0956	Control assembly
40	151-1059-F1	3-1/2 inch, 20 M, Hard disk drive with controller (ZWL-200-2)
	151-1058-F1	3-1/2 inch, 40 M, Hard disk drive with controller (ZWL-200-4)
41	969-1201	Spacer, nylon
42	969-0942	Cabinet,LCD back with shield
43	969-0965	Plug, line, tel, modem cover
44	969-0944	Back plate, main board
45	969-0953	Cabinet, keyboard
46	969-0962	Cabinet, bottom
47	969-0947	Cover, I/O ports
49	969-1193	Main PCB assembly
50	232-0127	Shield, hard drive
51	969-0950	Mounting pins, handle
52*	969-0952	Shield plate, LCD
53*	969-0963	Rubber foot
54	969-0964	Bracket, I/O port cover
55	969-0970	Cover, latch
56*	969-0978	Shield plate, main
57*	969-0987	Shield plate, keyboard
58	969-0994	Cable assembly, backlight
59	969-0995	Lithium cell
61	969-0992	Bracket, battery
62*	969-0967	Cushion
63	969-0971	Hook, right
64	969-0972	Hook, left
65	969-0973	Spring
66*	969-0974	Label, indication
67*	969-0980	Keyboard bracket, long
68*	969-0982	Keyboard bracket, short
69	969-0984	LCD bracket, left
71	969-0985	LCD bracket, right
72	969-0990	Spacer, left
73	969-0991	Spacer, right
74	969-0983	Bracket, cabinet
75	969-0988	Plate spring
76*	969-0975	Cover
77*	969-0993	Bracket, leaf switch
78*	969-0996	Leaf switch, lid

*Part must be ordered direct from vendor.

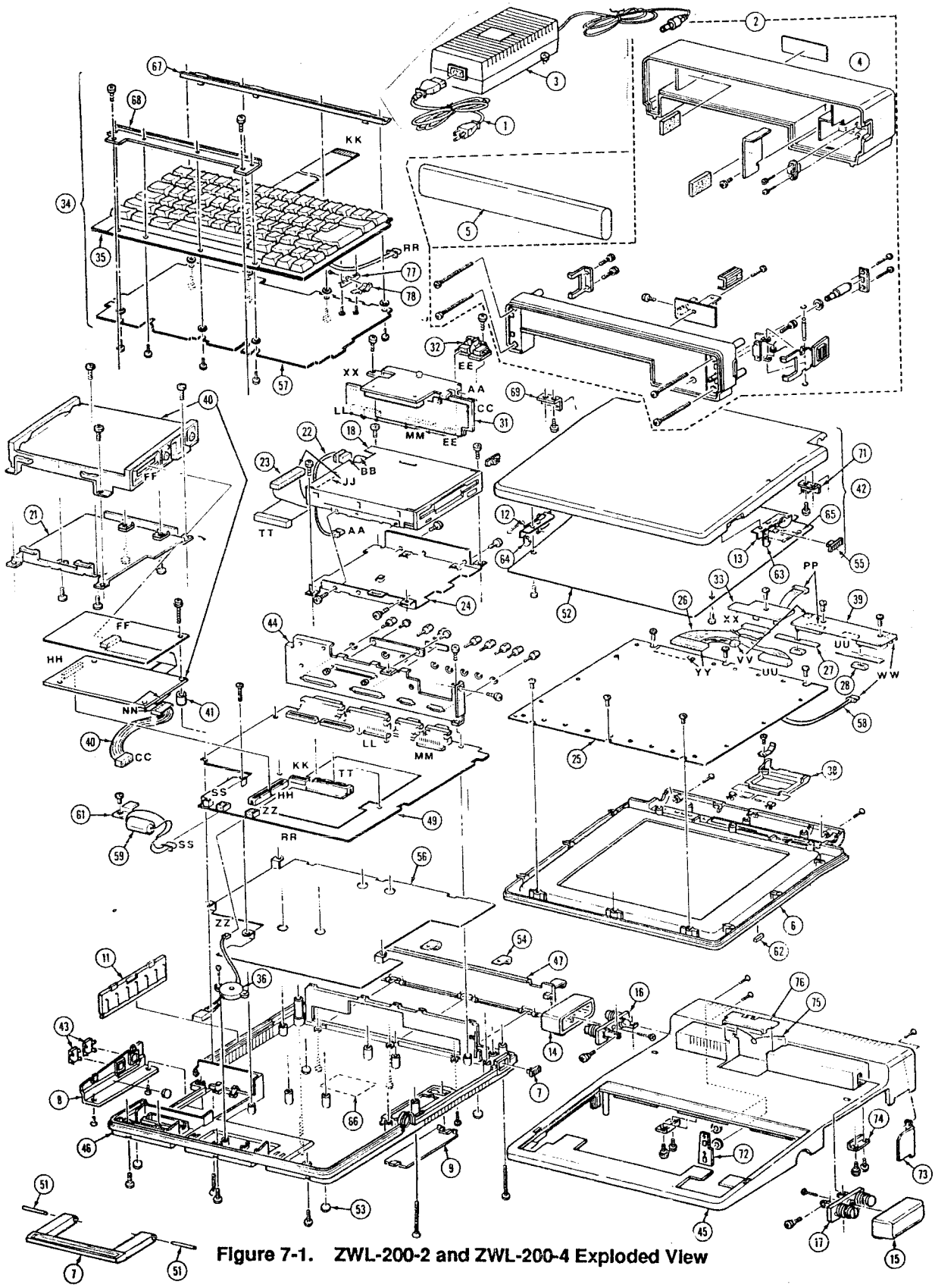


Figure 7-1. ZWL-200-2 and ZWL-200-4 Exploded View

Chapter 8
Schematics

This chapter contains the schematics for the ZWL-200-2/4 portable computer. Refer to Chapter 5 for circuit descriptions and to Figure 8-1 for illustrations of the schematic symbols used in this manual.

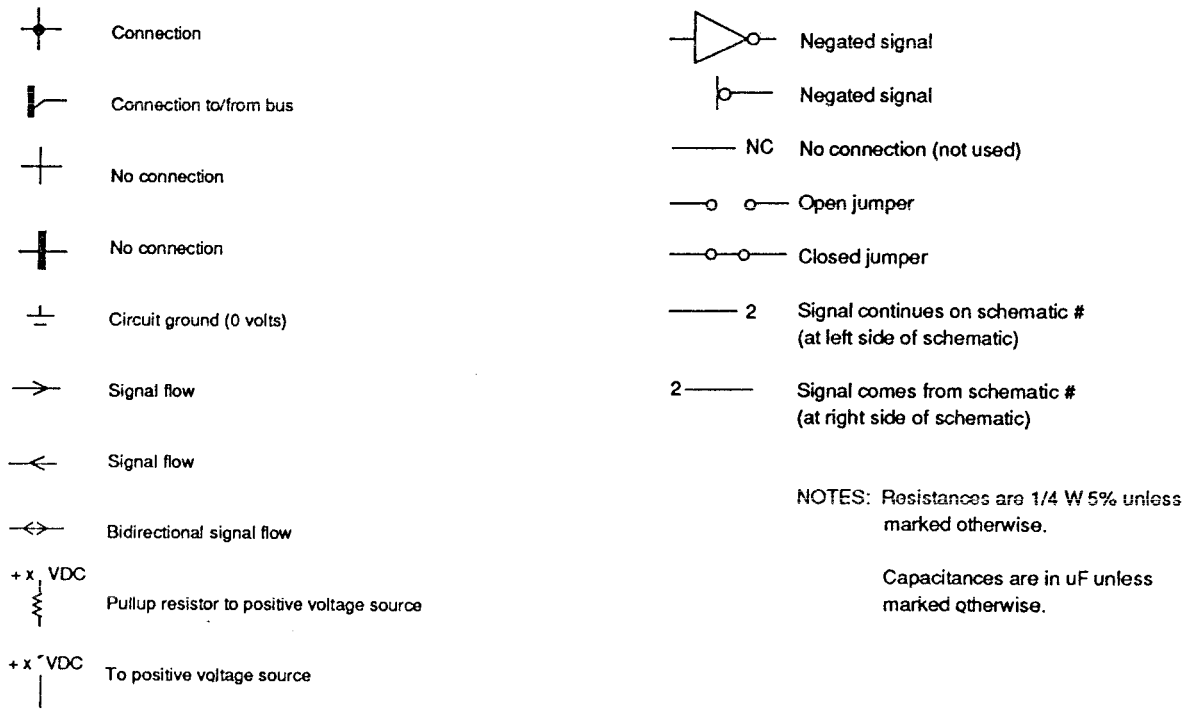
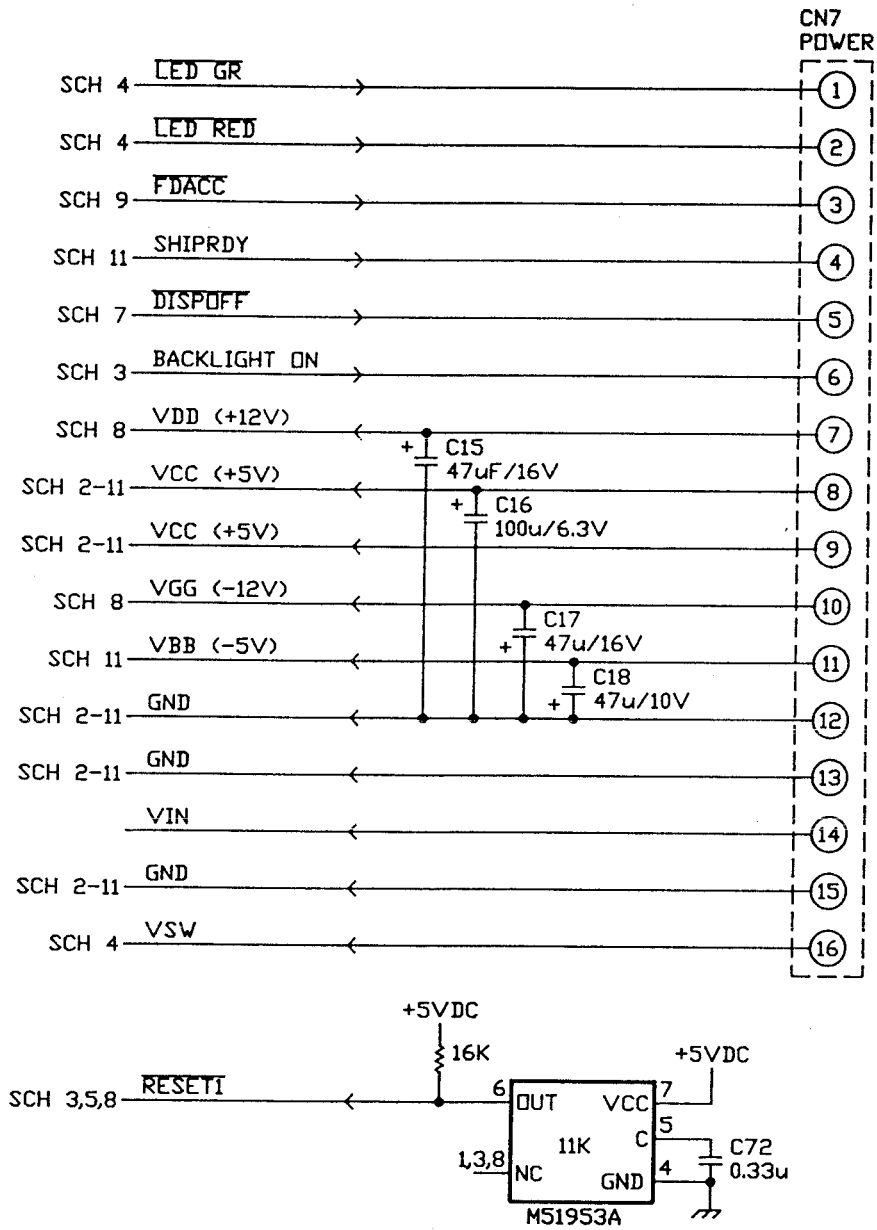
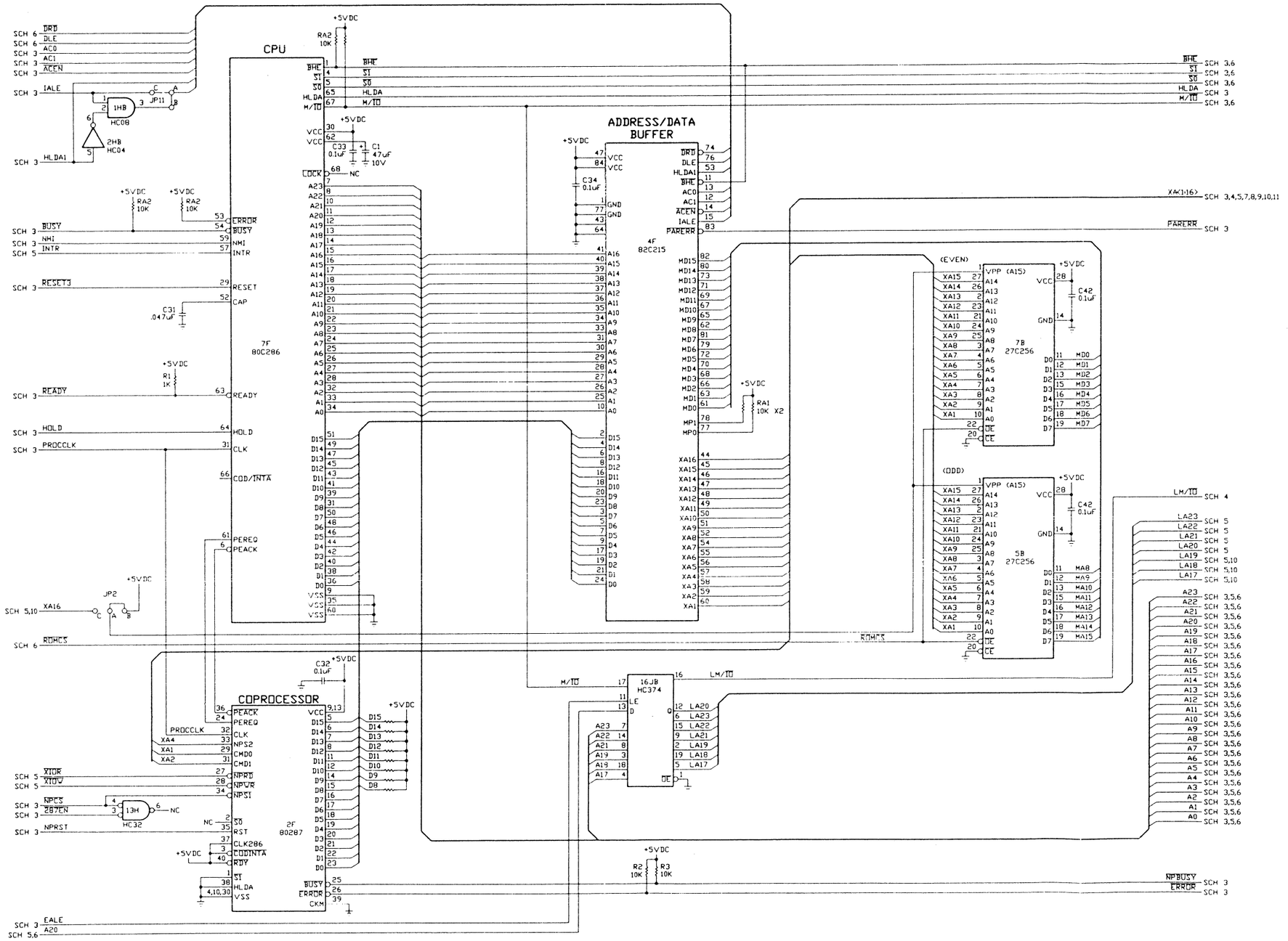


Figure 8-1. Schematic Symbols


CN7
POWER
SCH 4
LED GR
1
SCH 4
LED RED
2
SCH 9
FDACC
3
SCH 11
SHIPRDY
4
SCH 7
DISPOFF
5
SCH 3
BACKLIGHT ON
6
SCH 8
VDD (+12V)
7
C15
47uF/16V
SCH 2-11
VCC (+5V)
8
C16
100u/6.3V
SCH 2-11
VCC (+5V)
9
SCH 8
VGG (-12V)
10
C17
47u/16V
SCH 11
VBB (-5V)
11
C18
47u/10V
SCH 2-11
GND
12
SCH 2-11
GND
13
VIN
14
SCH 2-11
GND
15
SCH 4
VSW
16
+5VDC
16K
+5VDC
SCH 3,5,8
RESETI
6
OUT
VCC
7
5
11K
C
C72
0.33u
1,3,8
NC
GND
4
M51953A

Schematic 1


CPU
7F
80C286
ADDRESS/DATA
BUFFER
4F
82C215
COPROCESSOR
2F
80287
7B
27C256
5B
27C256
(EVEN)
(ODD)
16JB
HC374
1HB
HC08
2HB
HC04
13H
HC32
JP11
JP2
C33
0.1uF
C1
47uF
10V
C34
0.1uF
C42
0.1uF
C32
0.1uF
C31
.047uF
RA2
10K
RA1
10K X2
R1
1K
R2
10K
R3
10K
+5VDC
VCC
GND
NC
DRD
DLE
AC0
AC1
ACEN
IALE
HLDA1
BHE
SI
SO
HLDA
M/IO
CLOCK
BUSY
NMI
INTR
RESET
CAP
READY
HOLD
PROCCLK
CLK
COD/INTA
PEREQ
PEACK
ERROR
PAERR
XA(1-16)
LM/IO
LA23
LA22
LA21
LA20
LA19
LA18
LA17
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
MD15
MD14
MD13
MD12
MD11
MD10
MD9
MD8
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
MP1
MP0
XA16
XA15
XA14
XA13
XA12
XA11
XA10
XA9
XA8
XA7
XA6
XA5
XA4
XA3
XA2
XA1
RDHCS
XIOR
XIOW
NPRD
NPWR
NPSI
NPCS
287EN
NPRST
EALE
A20
NPBUSY
ERROR
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SCH 3
SCH 5,10
SCH 4
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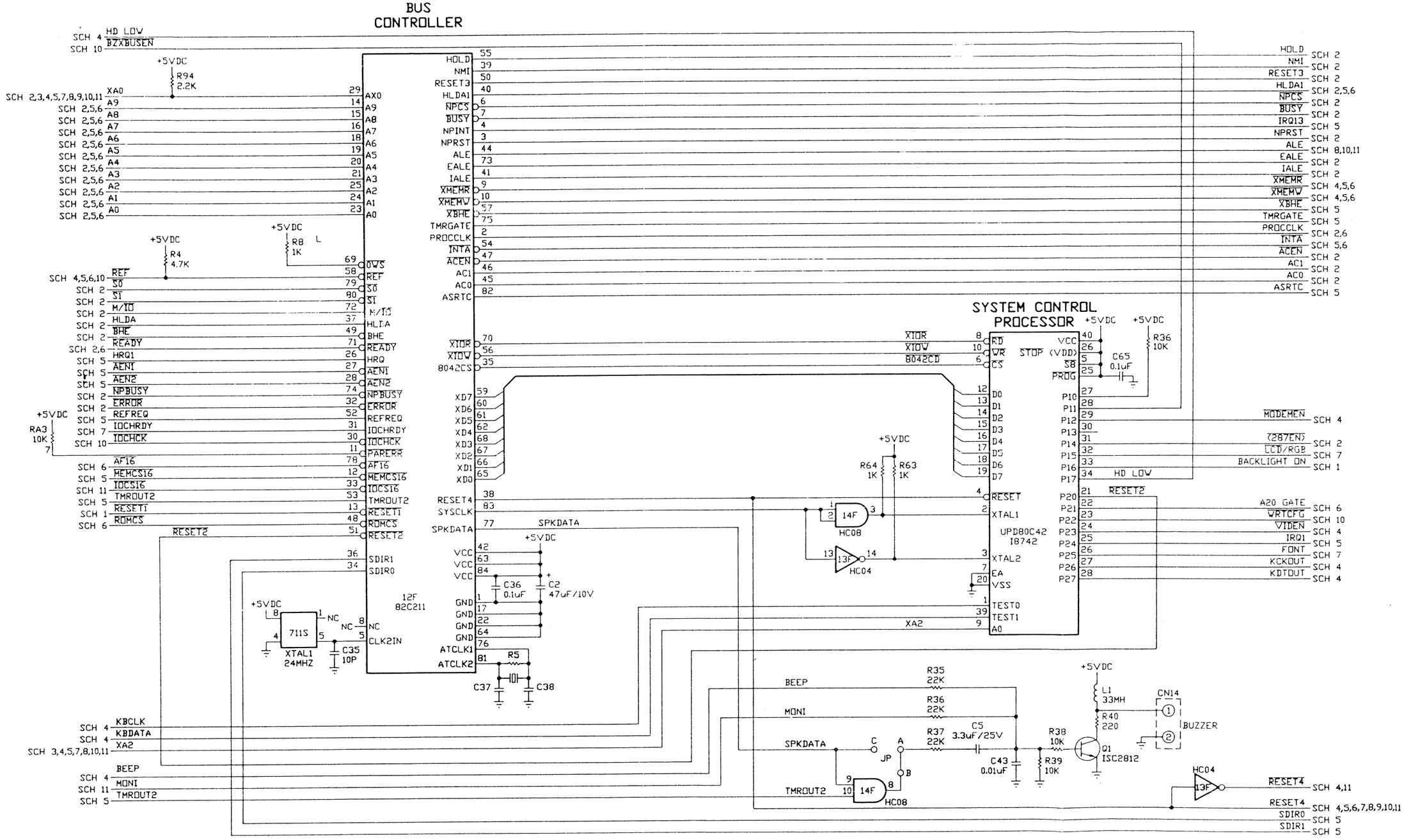
SCH 5
SCH 6
SCH 5,6

Schematic 2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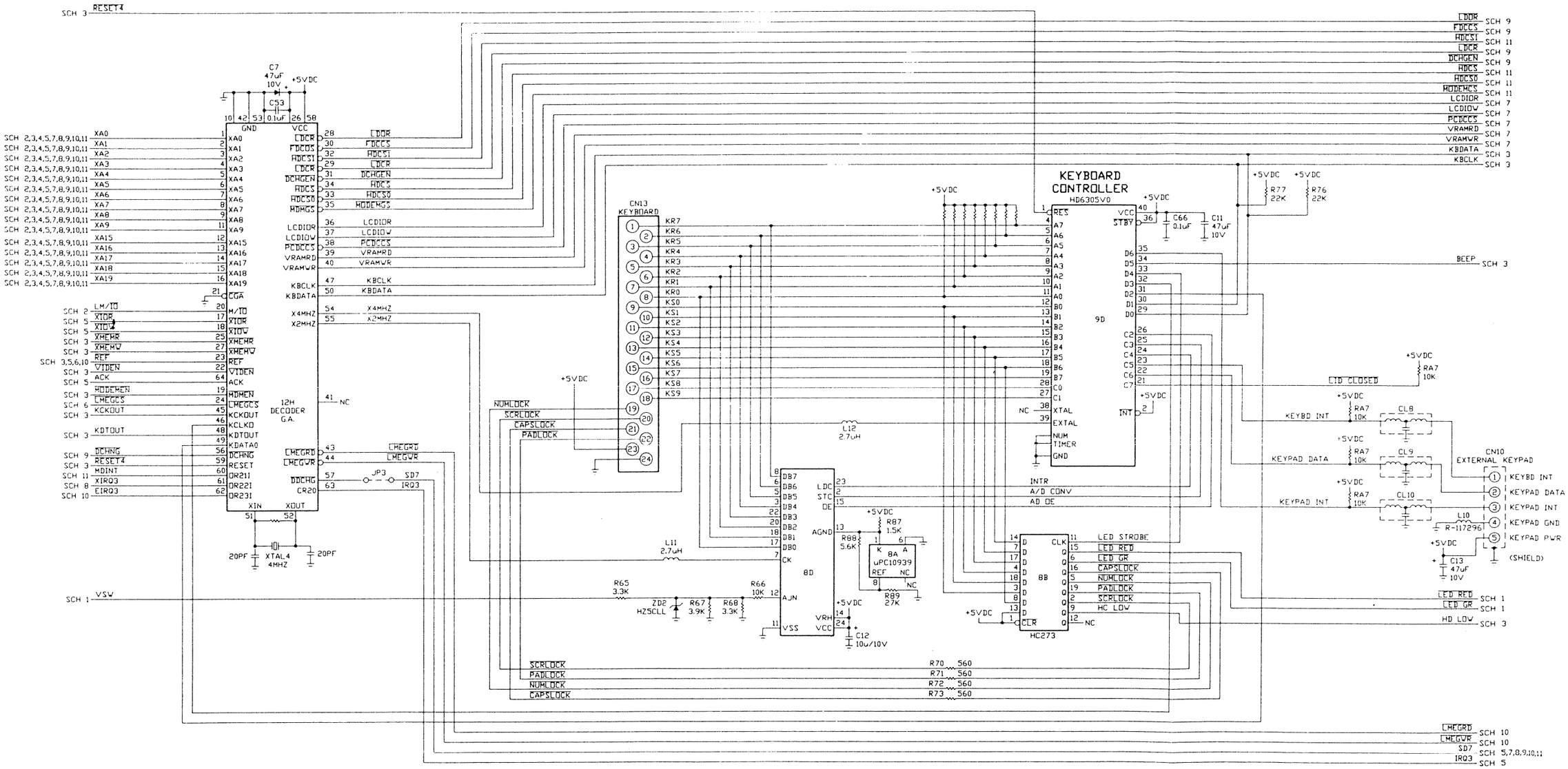
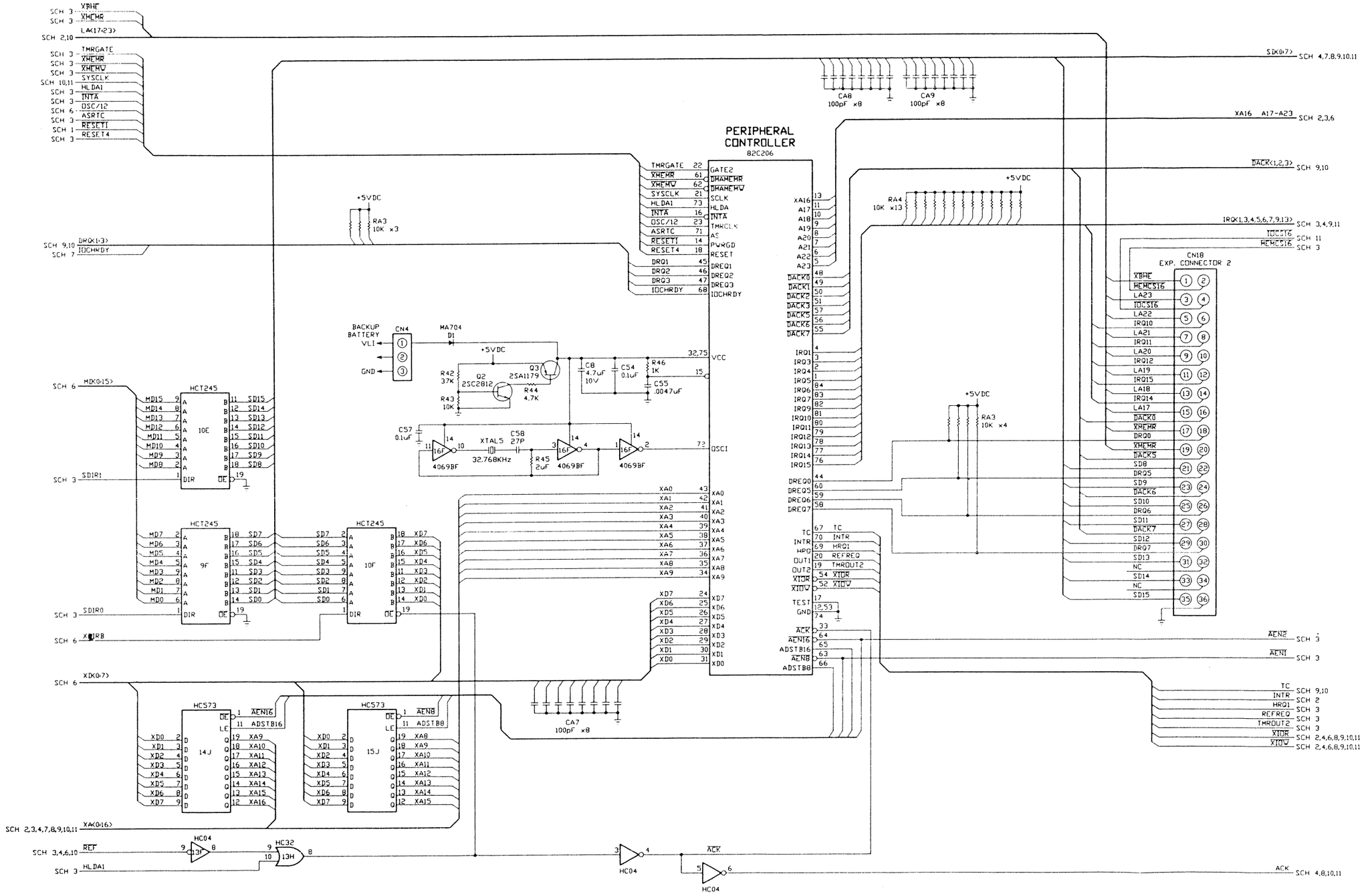
SYSTEM CONTROL PROCESSOR
UPD80C42 I8742
82C211
12F
HC08
HC04
711S
XTAL1 24MHZ
ISC2812
BUZZER
+5VDC
HD LOW
BZXBUSEN
RESET2
SPKDATA
BEEP
MONI
TMROUT2
XA2
R94 2.2K
R4 4.7K
R8 1K
RA3 10K
R64 1K
R63 1K
R5
R35 22K
R36 22K
R37 22K
R38 10K
R39 10K
R40 220
R36 10K
L1 33MH
C5 3.3uF/25V
C43 0.01uF
C65 0.1uF
C36 0.1uF
C2 47uF/10V
C35 10P
C37
C38
JP
CN14
HOLD
NMI
RESET3
HLDA1
NPCS
BUSY
NPINT
NPRST
ALE
EALE
IALE
XMEMR
XMEMW
XBHE
TMRGATE
PROCCLK
INTA
ACEN
AC1
AC0
ASRTC
XIOR
XIOW
8042CS
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
RESET4
SYSCLK
SDIR1
SDIR0
CLK2IN
ATCLK1
ATCLK2
REF
S0
S1
M/IO
HLDA
BHE
READY
HRQ1
AENI
AEN2
NPBUSY
ERROR
REFREQ
IOCHRDY
IOCHCK
PARERR
AF16
MEMCS16
IOCS16
TMROUT2
RESET1
ROMCS
RESET2
KBCLK
KBDATA
MODEMEN
(287EN)
LCD/RGB
BACKLIGHT ON
A20 GATE
WRTCFG
VIDEN
IRQ1
FONT
KCKOUT
KDTOUT
SCH 2,3,4,5,7,8,9,10,11 XA0
SCH 2,5,6 A9
SCH 2,5,6 A8
SCH 2,5,6 A7
SCH 2,5,6 A6
SCH 2,5,6 A5
SCH 2,5,6 A4
SCH 2,5,6 A3
SCH 2,5,6 A2
SCH 2,5,6 A1
SCH 2,5,6 A0
SCH 4,5,6,10 REF
SCH 2 S0
SCH 2 S1
SCH 2 M/IO
SCH 2 HLDA
SCH 2 BHE
SCH 2,6 READY
SCH 5 HRQ1
SCH 5 AENI
SCH 5 AEN2
SCH 2 NPBUSY
SCH 2 ERROR
SCH 5 REFREQ
SCH 7 IOCHRDY
SCH 10 IOCHCK
SCH 6 AF16
SCH 5 MEMCS16
SCH 11 IOCS16
SCH 5 TMROUT2
SCH 1 RESET1
SCH 6 ROMCS
SCH 4 KBCLK
SCH 4 KBDATA
SCH 3,4,5,7,8,10,11 XA2
SCH 4 BEEP
SCH 11 MONI
SCH 5 TMROUT2
SCH 4 HD LOW
SCH 10 BZXBUSEN
SCH 2 HOLD
SCH 2 NMI
SCH 2 RESET3
SCH 2,5,6 HLDA1
SCH 2 NPCS
SCH 2 BUSY
SCH 5 IRQ13
SCH 2 NPRST
SCH 8,10,11 ALE
SCH 2 EALE
SCH 2 IALE
SCH 4,5,6 XMEMR
SCH 4,5,6 XMEMW
SCH 5 XBHE
SCH 5 TMRGATE
SCH 2,6 PROCCLK
SCH 5,6 INTA
SCH 2 ACEN
SCH 2 AC1
SCH 2 AC0
SCH 5 ASRTC
SCH 4 MODEMEN
SCH 2 (287EN)
SCH 7 LCD/RGB
SCH 1 BACKLIGHT ON
SCH 6 A20 GATE
SCH 10 WRTCFG
SCH 4 VIDEN
SCH 5 IRQ1
SCH 7 FONT
SCH 4 KCKOUT
SCH 4 KDTOUT
SCH 4,11 RESET4
SCH 4,5,6,7,8,9,10,11 RESET4
SCH 5 SDIR0
SCH 5 SDIR1

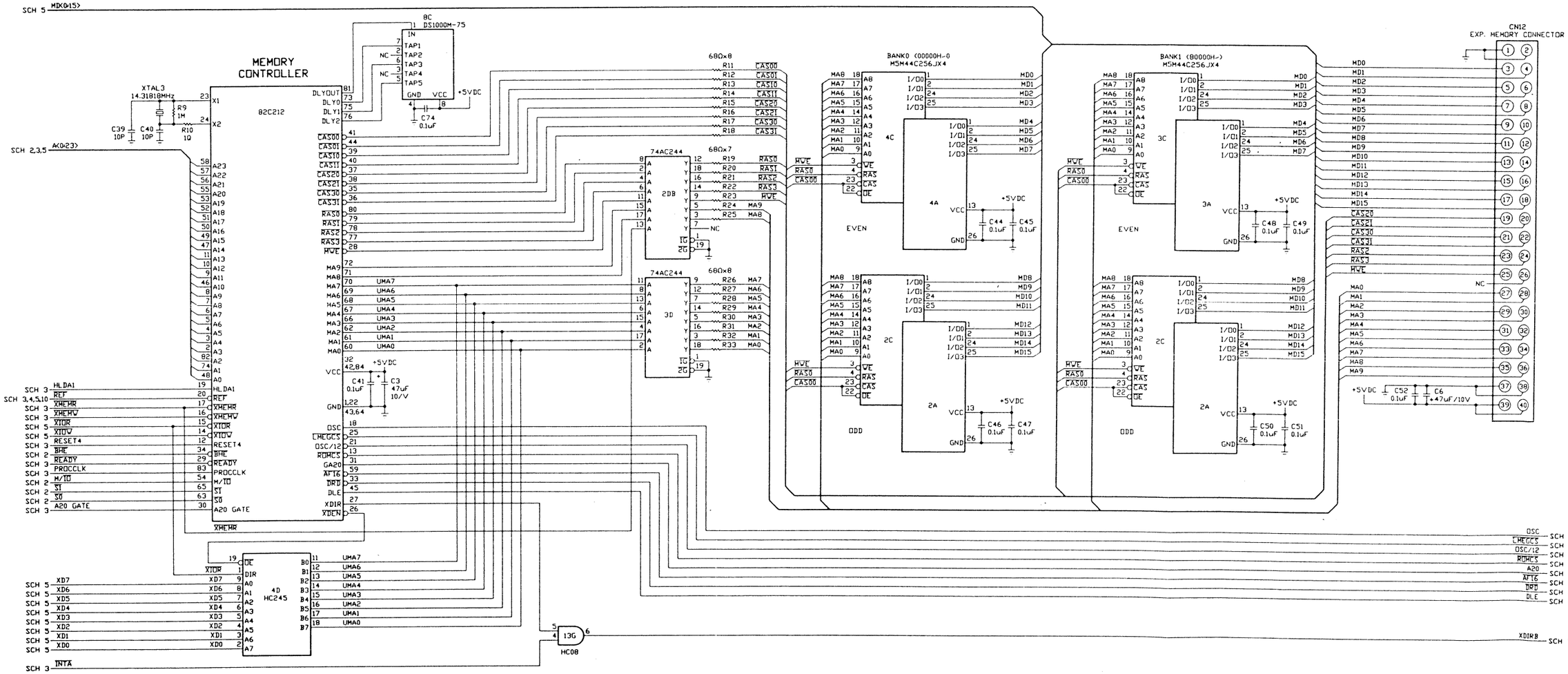
Schematic 3


KEYBOARD CONTROLLER
HD6305V0
CN13 KEYBOARD
12H DECODER G.A.
8D
8B
HC273
CN10 EXTERNAL KEYPAD
μPC10939
XTAL4 4MHZ
RESET4
VSW
+5VDC
LID CLOSED
KEYBD INT
KEYPAD DATA
KEYPAD INT
KEYPAD GND
KEYPAD PWR
(SHIELD)
BEEP
LED STROBE
LED RED
LED GR
CAPSLOCK
NUMLOCK
PADLOCK
SCRLOCK
HC LOW
HD LOW
INTR
A/D CONV
AD OE
LDDR
FDCCS
HDCS1
LDCR
DCHGEN
HDCS
HDCS0
MODEMCS
LCDIOR
LCDIOW
PCDCCS
VRAMRD
VRAMWR
KBDATA
KBCLK
LMEGRD
LMEGWR
SD7
IRQ3
VIDEN
ACK
MDINT
XIRQ3
EIRQ3
KDTOUT
KCKOUT
LMEGCS
MODEMEN
DCHNG
LM/IO
XIOR
XIOW
XMEMR
XMEMW
REF
X4MHZ
X2MHZ
NC
JP3

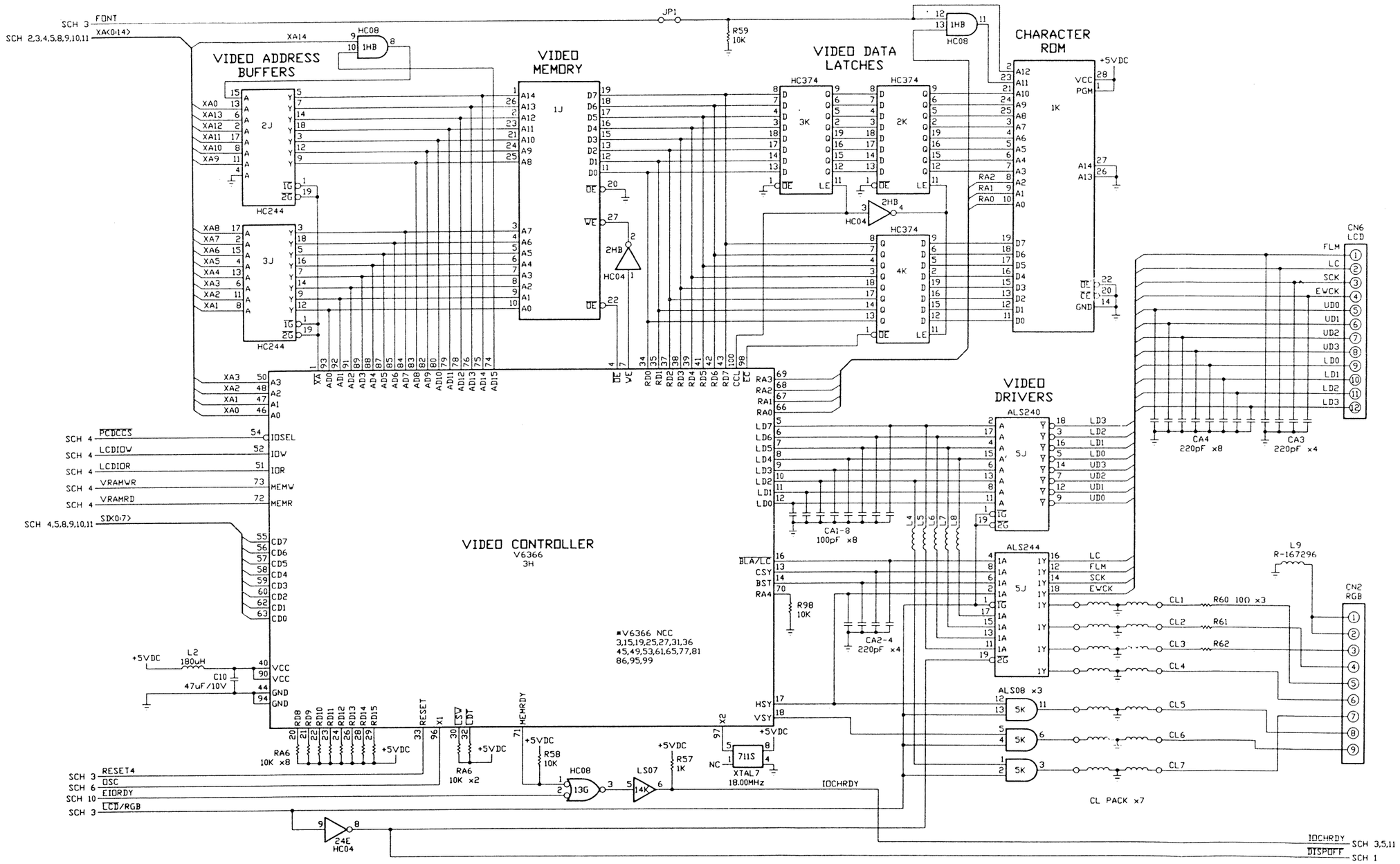
Schematic 4


PERIPHERAL CONTROLLER
82C206
HCT245
10E
9F
10F
HC573
14J
15J
CN4
BACKUP BATTERY
MA704
D1
Q3 2SA1179
Q2 2SC2812
XTAL5 32.768KHz
4069BF
CN18
EXP. CONNECTOR 2
+5VDC
CA8 100pF x8
CA9 100pF x8
CA7 100pF x8
RA3 10K x3
RA4 10K x13
RA3 10K x4
SDIR1
SDIR0
XDIRB
REF
HLDA1
ACK
SD(0-7)
XA16 A17-A23
DACK(1,2,3)
IRQ(1,3,4,5,6,7,9,13)
IOCS16
MEMCS16
AEN2
AEN1
TC
INTR
HRQ1
REFREQ
TMROUT2
XIOR
XIOW

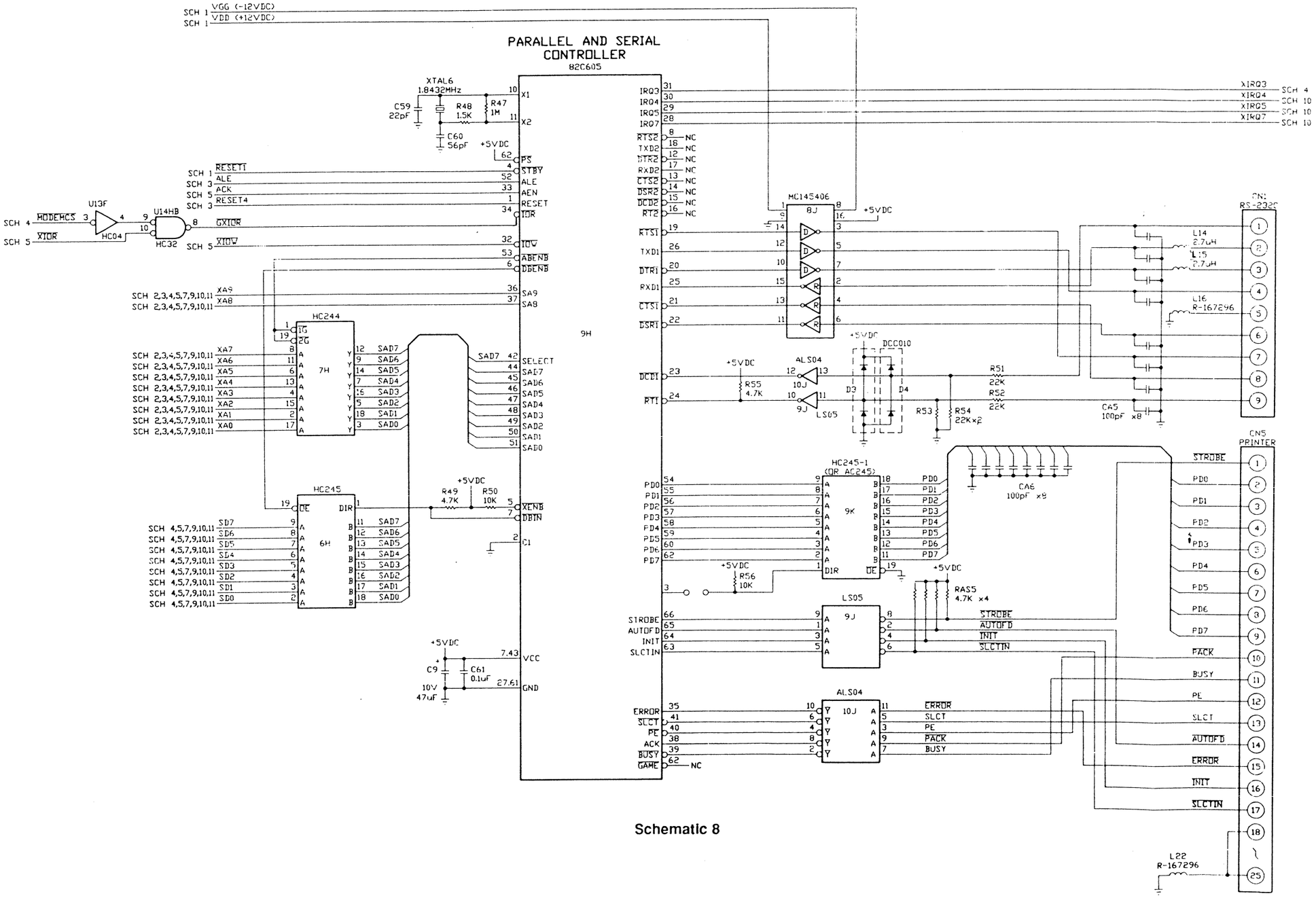
Schematic 5


MEMORY CONTROLLER
82C212
XTAL3
14.31818MHz
R9 1M
R10 1Ω
C39 10P
C40 10P
8C
DS1000M-75
C74 0.1uF
+5VDC
680x8
74AC244
2DB
3D
MA9
MA8
UMA7
UMA6
UMA5
UMA4
UMA3
UMA2
UMA1
UMA0
C41 0.1uF
C3 47uF 10/V
HC245
4D
HC08
BANK0 (00000H-0
M5M44C256JX4
BANK1 (80000H-)
M5M44C256JX4
4C
4A
3C
3A
2C
2A
EVEN
ODD
C44 0.1uF
C45 0.1uF
C46 0.1uF
C47 0.1uF
C48 0.1uF
C49 0.1uF
C50 0.1uF
C51 0.1uF
CN12
EXP. MEMORY CONNECTOR
C52 0.1uF
C6 +47uF/10V
SCH 5 MD<0:15>
SCH 2,3,5 A<0:23>
SCH 3 HLDA1
SCH 3,4,5,10 REF
SCH 3 XMEMR
SCH 3 XMEMW
SCH 5 XIOR
SCH 5 XIOW
SCH 3 RESET4
SCH 2 BHE
SCH 3 READY
SCH 3 PROCCLK
SCH 2 M/IO
SCH 2 S1
SCH 2 S0
SCH 3 A20 GATE
SCH 5 XD7
SCH 5 XD6
SCH 5 XD5
SCH 5 XD4
SCH 5 XD3
SCH 5 XD2
SCH 5 XD1
SCH 5 XD0
SCH 3 INTA
OSC
CMEGCS
OSC/12
ROMCS
A20
AT16
DRD
DLE
XDIRB
SCH 7
SCH 4
SCH 5
SCH 2,3
SCH 2,3
SCH 6
SCH 2
SCH 2
SCH 5

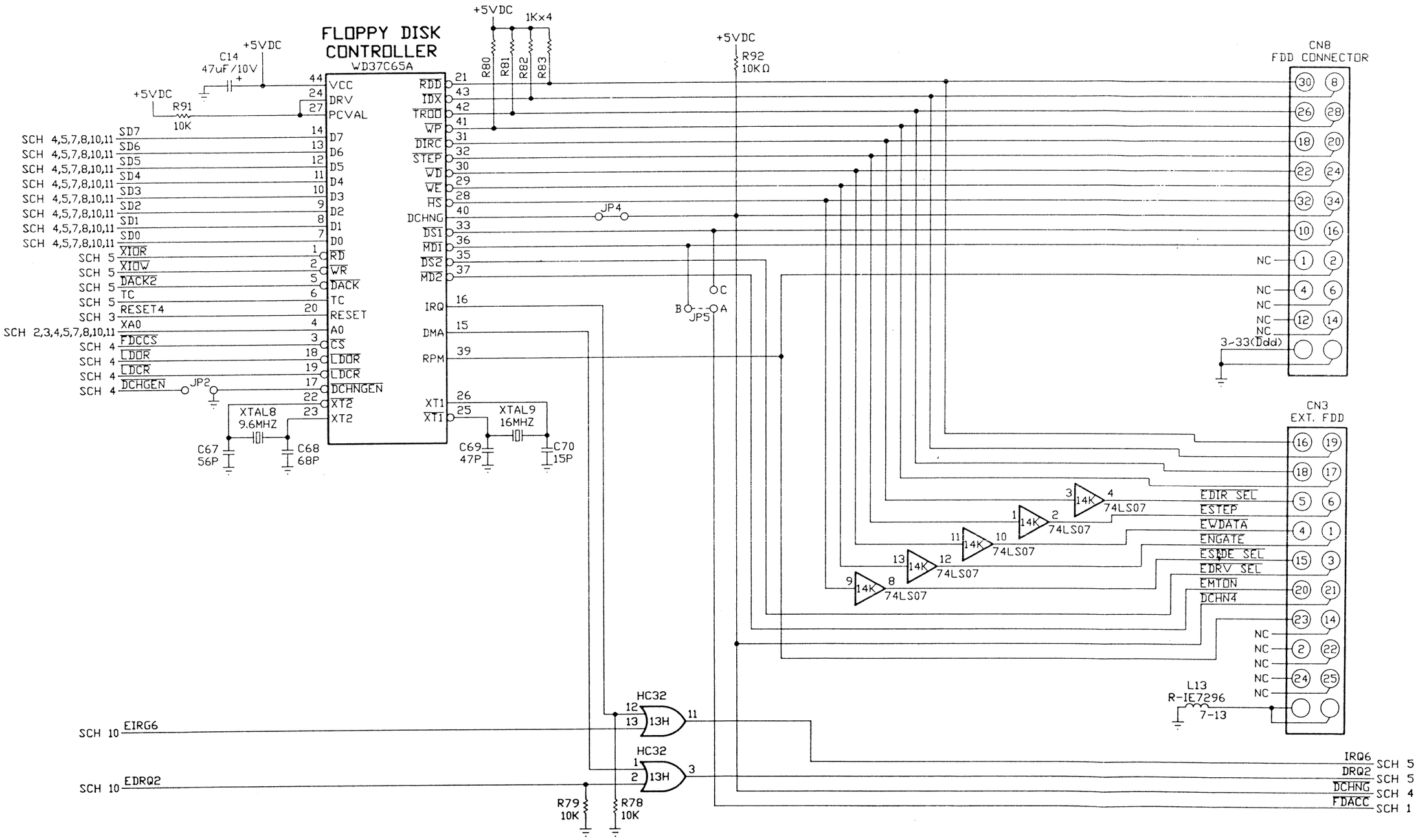
Schematic 6


VIDEO ADDRESS BUFFERS
VIDEO MEMORY
VIDEO DATA LATCHES
CHARACTER ROM
VIDEO DRIVERS
VIDEO CONTROLLER
V6366
3H
SCH 3 FONT
SCH 2,3,4,5,8,9,10,11 XA<0:14>
JP1
R59 10K
HC08
HC244
HC374
HC04
2HB
1HB
2J
3J
1J
3K
2K
4K
1K
5J
+5VDC
VCC
PGM
GND
CN6 LCD
FLM
LC
SCK
EWCK
UD0
UD1
UD2
UD3
LD0
LD1
LD2
LD3
CA4 220pF x8
CA3 220pF x4
CA1-8 100pF x8
CA2-4 220pF x4
ALS240
ALS244
ALS08 x3
5K
CL1
CL2
CL3
CL4
CL5
CL6
CL7
R60 10Ω x3
R61
R62
L9 R-167296
CN2 RGB
CL PACK x7
SCH 4 PCDCCS
SCH 4 LCDIOW
SCH 4 LCDIOR
SCH 4 VRAMWR
SCH 4 VRAMRD
SCH 4,5,8,9,10,11 SD<0:7>
IOSEL
IOW
IOR
MEMW
MEMR
CD7
CD6
CD5
CD4
CD3
CD2
CD1
CD0
L2 180uH
C10 47uF/10V
RA6 10K x8
RA6 10K x2
R98 10K
R58 10K
R57 1K
LS07
14K
HC08
13G
711S
XTAL7
18.00MHz
24E
HC04
■V6366 NCC
3,15,19,25,27,31,36
45,49,53,61,65,77,81
86,95,99
SCH 3 RESET4
SCH 6 OSC
SCH 10 EIORDY
SCH 3 LCD/RGB
IOCHRDY
SCH 3,5,11 IOCHRDY
SCH 1 DISPOFF

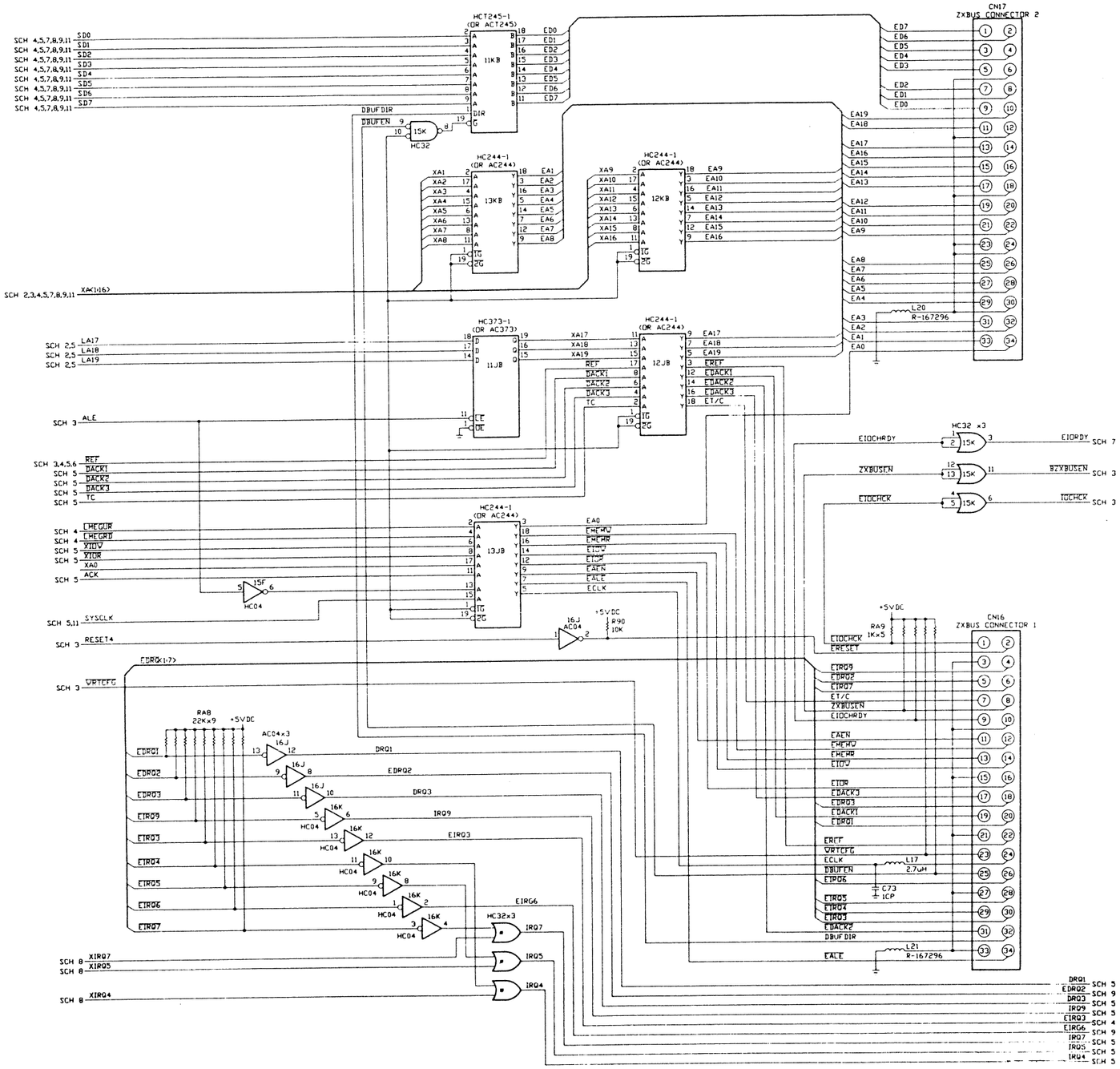
Schematic 7


PARALLEL AND SERIAL CONTROLLER
82C605
VGG (-12VDC)
VDD (+12VDC)
XTAL6
1.8432MHz
C59
22pF
R48
1.5K
R47
1M
C60
56pF
+5VDC
X1
X2
PS
STBY
ALE
AEN
RESET
IOR
IOW
ABENB
DBENB
SA9
SA8
SELECT
SAD7
SAD6
SAD5
SAD4
SAD3
SAD2
SAD1
SAD0
XCNB
DBIN
C1
VCC
GND
9H
IRQ3
IRQ4
IRQ5
IRQ7
XIRQ3
XIRQ4
XIRQ5
XIRQ7
RTS2
TXD2
DTR2
RXD2
CTS2
DSR2
DCD2
RI2
NC
MC145406
8J
RTS1
TXD1
DTR1
RXD1
CTS1
DSR1
DCD1
RI1
DCC010
D3
D4
R51
22K
R52
22K
R53
R54
22K×2
R55
4.7K
ALS04
10J
9J
LS05
CN1
RS-232C
L14
2.7uH
L15
2.7uH
L16
R-167296
CA5
100pF x8
HC244
7H
HC245
6H
SCH 1 RESET1
SCH 3 ALE
SCH 5 ACK
SCH 3 RESET4
SCH 4 MODEMCS
SCH 5 XIOR
U13F
HC04
U14HB
HC32
GXIOR
SCH 5 XIOW
SCH 2,3,4,5,7,9,10,11 XA9
SCH 2,3,4,5,7,9,10,11 XA8
SCH 2,3,4,5,7,9,10,11 XA7
SCH 2,3,4,5,7,9,10,11 XA6
SCH 2,3,4,5,7,9,10,11 XA5
SCH 2,3,4,5,7,9,10,11 XA4
SCH 2,3,4,5,7,9,10,11 XA3
SCH 2,3,4,5,7,9,10,11 XA2
SCH 2,3,4,5,7,9,10,11 XA1
SCH 2,3,4,5,7,9,10,11 XA0
SCH 4,5,7,9,10,11 SD7
SCH 4,5,7,9,10,11 SD6
SCH 4,5,7,9,10,11 SD5
SCH 4,5,7,9,10,11 SD4
SCH 4,5,7,9,10,11 SD3
SCH 4,5,7,9,10,11 SD2
SCH 4,5,7,9,10,11 SD1
SCH 4,5,7,9,10,11 SD0
R49
4.7K
R50
10K
C9
10V
47uF
C61
0.1uF
HC245-1
(OR AC245)
9K
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
R56
10K
CA6
100pF x9
RA55
4.7K x4
STROBE
AUTOFD
INIT
SLCTIN
ERROR
SLCT
PE
ACK
BUSY
PACK
GAME
CN5
PRINTER
L22
R-167296

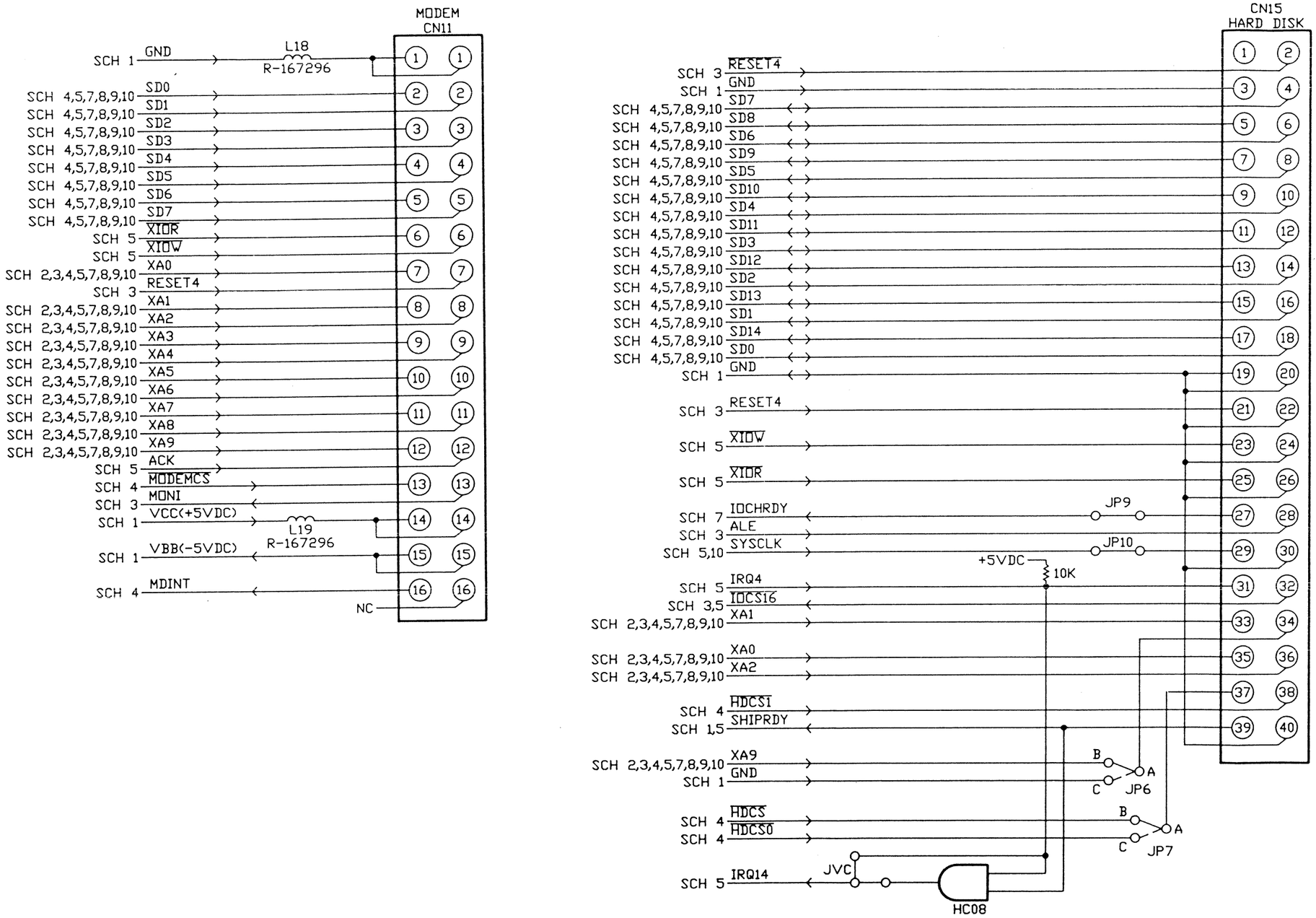
Schematic 8


FLOPPY DISK CONTROLLER
WD37C65A
+5VDC
C14
47uF/10V
R91
10K
1K×4
R80
R81
R82
R83
R92
10KΩ
JP4
JP5
JP2
XTAL8
9.6MHZ
XTAL9
16MHZ
C67
56P
C68
68P
C69
47P
C70
15P
VCC
DRV
PCVAL
D7
D6
D5
D4
D3
D2
D1
D0
RD
WR
DACK
TC
RESET
A0
CS
LDOR
LDCR
DCHNGEN
XT2
XT1
RDD
IDX
TROO
WP
DIRC
STEP
WD
WE
HS
DCHNG
DS1
MD1
DS2
MD2
IRQ
DMA
RPM
SCH 4,5,7,8,10,11 SD7
SCH 4,5,7,8,10,11 SD6
SCH 4,5,7,8,10,11 SD5
SCH 4,5,7,8,10,11 SD4
SCH 4,5,7,8,10,11 SD3
SCH 4,5,7,8,10,11 SD2
SCH 4,5,7,8,10,11 SD1
SCH 4,5,7,8,10,11 SD0
SCH 5 XIOR
SCH 5 XIOW
SCH 5 DACK2
SCH 5 TC
SCH 3 RESET4
SCH 2,3,4,5,7,8,10,11 XA0
SCH 4 FDCCS
SCH 4 LDOR
SCH 4 LDCR
SCH 4 DCHGEN
SCH 10 EIRG6
SCH 10 EDRQ2
HC32
13H
R79
10K
R78
10K
CN8
FDD CONNECTOR
NC
3-33(Ddd)
CN3
EXT. FDD
L13
R-IE7296
7-13
74LS07
EDIR SEL
ESTEP
EWDATA
ENGATE
ESIDE SEL
EDRV SEL
EMTON
DCHN4
NC
IRQ6
DRQ2
DCHNG
FDACC
SCH 5
SCH 5
SCH 4
SCH 1

Schematic 9



Schematic 10



Schematic 11

SERVICE MANUAL ADDENDUM

Portable Computer

ZWL-200-2/4

ZENITH data systems

584-44

860-197

How to Use This Addendum

This addendum affects the following ZDS service documents:

- ZWL-200-2/4 Portable Computer Service Manual (585-295/860-197)

It reflects the change of the CPU processor to the Intel 80286 at Sanyo unit 651, design changes occuring at Sanyo unit 1001 and changes to the setup program at ROM version 2.3C.

Pages printed on white paper are replacement pages, they contain new information that applies to all units since initial production. Remove the original pages from your manual and replace them with the white pages supplied with this addendum.

Pages printed on gold paper have new information that applies to the units mentioned above. The new information is printed in italics and a symbol (*) is placed next to it. Remove the gold pages from this document and insert then in the appropriate places in the service document. The page number at the bottom of each addendum page indicates where to insert it. For example, if the first page of the addendum is 4-1A, insert it and the consecutive pages of the addendum between pages 4-2 and 4-3 in the service document.

Do not remove any previous addendum pages from the service document.

internal LEDs to report the status of these tests, but the tests include the same tests in the same sequence used in other Zenith computers. If the computer completes these tests successfully, it attempts to boot the disk installed in drive A.

After approximately five seconds, the screen will blink and the disk access LED for drive A will light. On initial power-up, the system will attempt to boot drive A. If there is no disk in drive A, the computer will attempt to boot to the default partition of the hard disk. You can defeat autoboot or change the autoboot procedure on the SupersPort computer by changing an entry in the Setup/Configuration menu, refer to Chapter 4 for information on the Setup/Configuration menu. You can also abort or bypass the autoboot sequence by pressing the ESC key after the boot sequence has started. When you bypass the autoboot sequence, the Monitor prompt (->) will appear on the screen.

If a disk is not installed in drive A, the computer will attempt to load the operating system from the default partition of the hard drive. If the default partition does not contain an operating system, an error message will appear. You can then reset the computer to the Monitor program by pressing the ESC key. If the default partition contains an operating system, the system will complete the boot-up operation.

If the computer completes all operations normally, the computer will load the operating system. You can now load disk-based test software to continue testing the system. You can reset the computer at any time by pressing CTRL-ALT-DEL. This restarts the power-up and autoboot sequence. You can reset the computer to the Monitor program by pressing CTRL-ALT-INS.

After testing the computer, use the following steps to power down the computer. This sequence prevents accidental damage that could extend your service time and costs.

1. Remove all disks.

2. Turn off the power to conserve battery power and prevent unintended operation of the computer.

3. Close and latch the computer to stabilize the cabinet.

80287 Coprocessor Installation

The SupersPort computer supports an 80287 coprocessor. To install a numeric coprocessor:

1. Turn the computer off. If the external AC power supply is attached to the computer, disconnect it.

2. Close and latch the lid.

3. Place a soft cloth on your work surface and turn the computer upside down on your work surface.

4. Carefully pry up on the coprocessor cover, as shown in Figure 2-4.

CAUTION

ICs are complex electronic devices that can be damaged by static electricity. Once you remove the IC from its protective foam packing, do not lay the IC down or let go of it until it is installed in its socket.

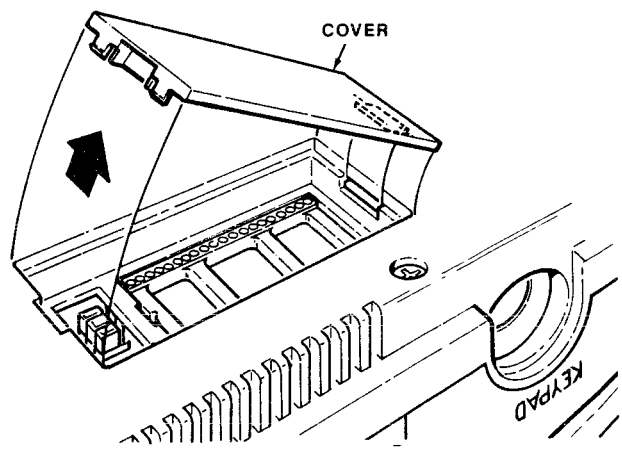


Figure 2-4. Removing the Coprocessor Cover

5. Carefully install the 80287 coprocessor IC. Press the IC firmly into the socket.

NOTE: A pin can become bent under the IC and will appear to be correctly seated in its socket. If a malfunction occurs while testing, examine the IC (and remove it, if necessary) to be certain that all pins are correctly inserted.

6. Replace the coprocessor cover.

Battery Operation

The SupersPort 286 computer uses a rechargeable nickel-cadmium battery for portable operation. The length of time the computer will operate with the battery depends upon the computer's features and the battery's capabilities.

Installation

Use the following procedure for installing the optional battery pack on the computer. You do not need any special tools. Refer to Figure 2-5 for the following steps.

1. Position the battery pack as shown in the figure.
2. Insert the battery pack hooks labeled A into the holes in the back of the computer.
3. Rotate the battery pack toward the computer until the guide post enters its receptacle in the computer.
4. Press the battery pack button and insert the hooks labeled B into the holes in the computer.
5. Release the button and press in on the battery pack until it locks in place.

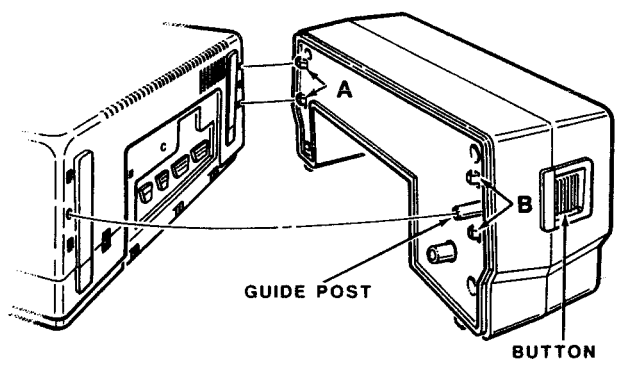


Figure 2-5. Battery Pack Installation

Removal

Use the following procedure for removing the optional battery pack from the computer.

1. Depress the battery pack button and rotate the button end away from the computer.
2. Remove the hooks labeled A from the holes in the back of the computer.

Battery Care

Nickel-cadmium batteries have three unique operating characteristics:

1. They are rechargeable.
2. They maintain a constant voltage level over their operating period. (Carbon or alkaline batteries do not maintain this constant voltage level. Instead, their output gradually drops.)
3. They can develop a severely reduced operating period if you do not care for them properly.

To get the most use from the battery:

- Keep disk drive use to a minimum. Some programs use a lot of disk input/output. For these programs, set up a virtual disk (sometimes called a RAM disk or memory disk). Refer to your operating system documentation for more information on virtual disks.
- Keep the display backlight set to the lowest level possible for comfortable operation. In some situations, natural light will be enough for normal operation without the backlight. This is particularly true in bright sunlight.
- Operate the battery as long as possible before recharging it. When the battery power is low, the power LED turns red. You then have about ten minutes to complete and save your work.
- Allow the computer to operate until the battery is completely dead (the backlight ceases to function and the screen data becomes garbled).

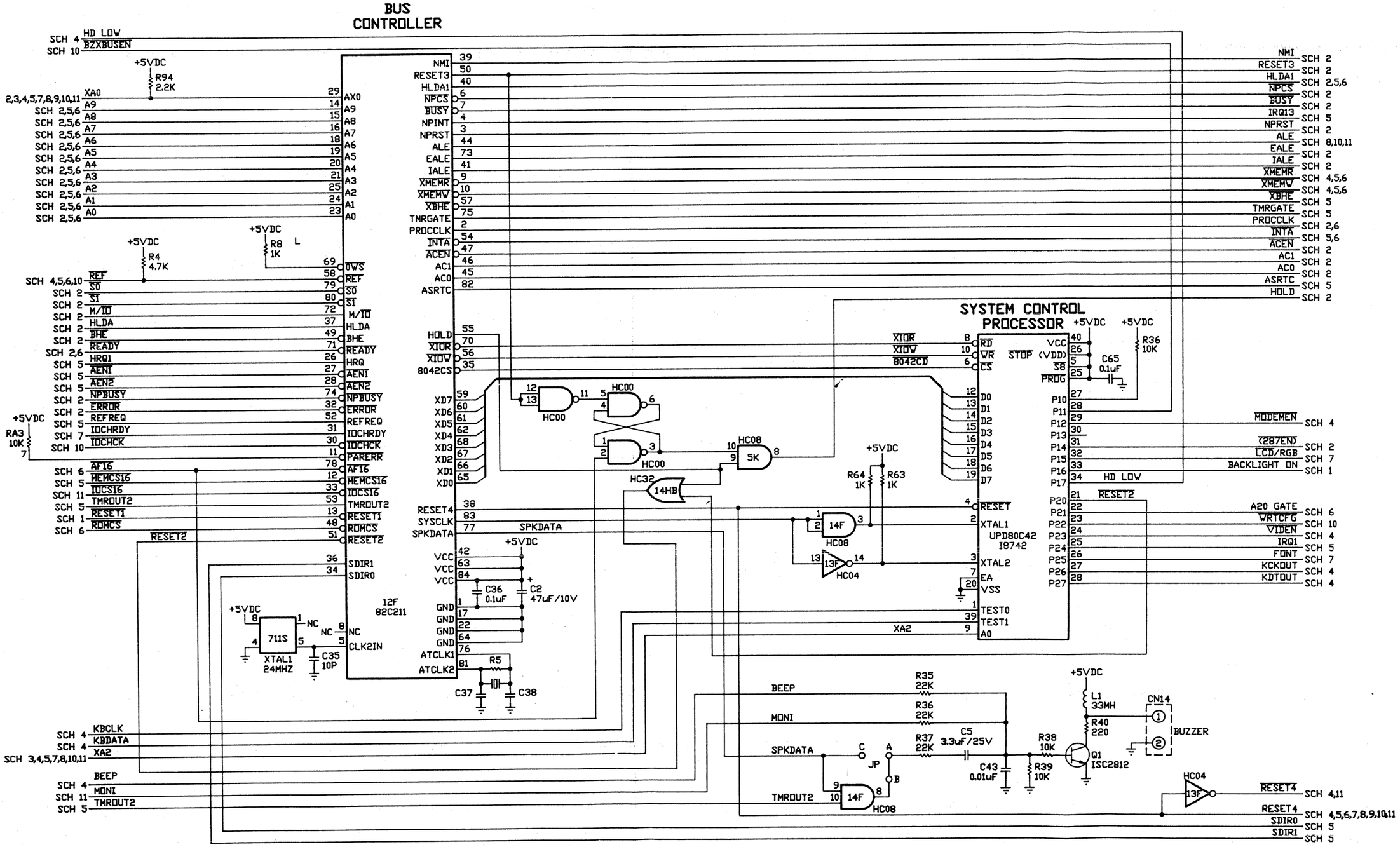
- Charge the battery for eight to twelve hours. If you are using the quick-charge battery pack, you will only have to charge it for one to two hours.

Audible Alarm

When the battery becomes low, the power LED will begin flashing red and the keyboard beeper will begin sounding an audible alarm. The audible alarm can be turned off by pressing and holding the FN key and then pressing the space bar.

Should the battery return to a normal operating level and then again decrease until the power LED again begins flashing the audible alarm will again begin to sound.

If the audible alarm has been turned off and the battery discharges to a seriously low level, the audible alarm will again sound. The audible alarm can again be turned off using the FN-space bar combination.



Schematic 3A

Chapter 4
Configuration

This chapter describes the Setup/Configuration menu and the display font selection jumpers used in this computer.

Setup/Configuration Menu

The Setup/Configuration menu serves as a reference for the computer by storing information about its configuration in a special CMOS memory device.The information must be changed if you alter the computer's configuration. To run the program, press the CTRL-ALT-INS key combination to drive the computer to the Monitor program. Type SETUP at the Monitor prompt (-->) and press ENTER.

The Setup/Configuration menu display consists of two screens. One displays the hardware information when the computer is used as a portable, that is, when the optional expansion chassis is not attached to the computer. This screen displays the message `Expansion Chassis Not Installed`. The other screen displays hardware information when the optional expansion chassis is attached. This screen displays the message `Expansion Chassis Installed`. You can change from one screen to the other with the Fn-PgUp and Fn-PgDn keys. Each screen may contain different information.

When the Setup/Configuration program screen appears, the active selection in each field is highlighted with a rectangular, reverse-video image, as shown in Figure 4-1.

Use the cursor control keys to move to the fields in the menu. Use the space bar and BACK SPACE key to move between entries within each field, except the time, date, Wini Powerdown, and Backlight fields. These fields must be typed in and entered using the ENTER key. To make a selection in the remaining fields, move to the desired field and highlight the entry that describes the computer. The selection will be locked in when you move to the next field. The message area at the bottom of the screen will provide help and error messages.

Figure 4-1 shows the default, or factory set, entries for the `Expansion Chassis Not Installed` screen. The default entries for the `Expansion Chassis Installed` screen are the same. However, each screen can contain different entries.

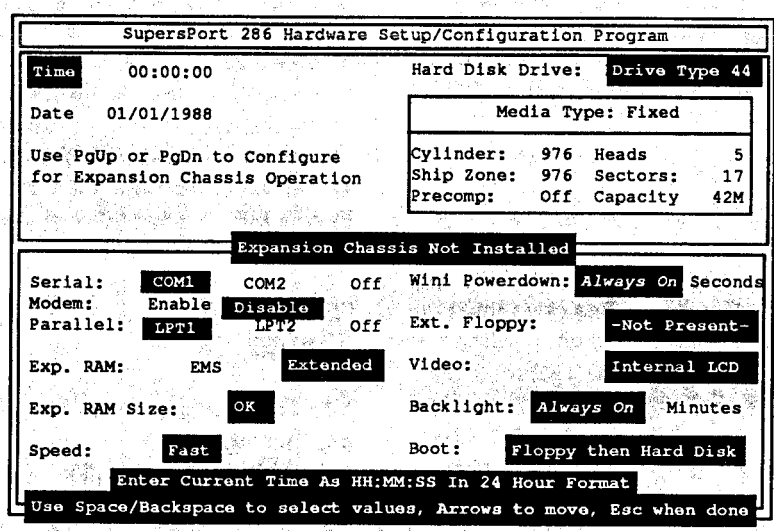

SupersPort 286 Hardware Setup/Configuration Program
Time 00:00:00
Date 01/01/1988
Use PgUp or PgDn to Configure for Expansion Chassis Operation
Hard Disk Drive: Drive Type 44
Media Type: Fixed
Cylinder: 976 Heads 5
Ship Zone: 976 Sectors: 17
Precomp: Off Capacity 42M
Expansion Chassis Not Installed
Serial: COM1 COM2 Off
Modem: Enable Disable
Parallel: LPT1 LPT2 Off
Exp. RAM: EMS Extended
Exp. RAM Size: OK
Speed: Fast
Wini Powerdown: Always On Seconds
Ext. Floppy: -Not Present-
Video: Internal LCD
Backlight: Always On Minutes
Boot: Floppy then Hard Disk
Enter Current Time As HH:MM:SS In 24 Hour Format
Use Space/Backspace to select values, Arrows to move, Esc when done

Figure 4-1. Setup/Configuration Menu Screen

The computer's clock and calendar are battery-operated and will run continuously, even when the computer is turned off. To keep accurate time, you must set the time and date when you turn on the computer for the first time. After that, you only need to enter a new time and date if you replace the backup battery.

Time

The computer keeps track of time using a 24-hour clock, in hours (00-23), minutes (00-59), and seconds (00-59). Type in the time of day using this format, and then press the ENTER key. For example, to enter 8:35 a.m., type 083500; to enter 8:35 p.m. type 203500. The computer automatically adds the colons (:) to separate the hours, minutes, and seconds.

If you make a mistake while typing, use the BACKSPACE key to erase the incorrect entry, type it again, and then press the ENTER key.

Date

The computer keeps track of the date using months (1-12), days (1-31), and years. Type in the date using this format, then press the ENTER key. For example, to set the calendar for January 5, 1988, type 01051988. The computer automatically adds the slashes (/) to seperate the month, day, and year.

Again, if you make a mistake while typing, use the BACKSPACE key to erase the incorrect entry, type it again, and then press the ENTER key.

Hard Disk Drive

When the computer is shipped from the factory, the hard disk drive type is set to match the drive that was installed in the computer. You should not change this selection unless the original drive is replaced by a drive of a different type. If the backup battery is replaced, the drive type will have to be re-entered. Press the spacebar to step through the drive types.

Serial

The serial port can be addressed as either COM1 or COM2. If there is no serial device attached to the computer, the serial port can be turned off. Setting the serial port off conserves power during battery operation.

Modem

The modem, if present, can be enabled or disabled. Disabling the modem conserves power during battery operation.

Parallel

The parallel field determines whether the parallel port is addressed as LPT1 or LPT2. Turning the parallel port off conserves battery power.

Expansion RAM

The Expansion RAM field determines whether the expansion memory will be used as EMS memory or extended memory.

Expansion RAM Size

If your computer contains more than 1 megabyte of memory, you need to select the number of kilobytes of expansion memory you have added to the system. The selections *are 0K, 1024K, and 4096K.* Use the ✶ space bar to increase the number and the BACKSPACE key to choose a lower number. If you do not have any expansion memory, select 0K.

Speed

You have a choice of three speed modes: slow, fast, and smart. The fast speed is the normal (and default) mode of operation. However, some programs

may require a slower speed in order to run. The smart mode slows the computer down for floppy disk drive operations but allows the fast speed for other operations. If the program still does not run properly, it may require the slow mode. This mode slows down all CPU and Memory operations of the computer. Bus speed remains fixed at 6MHz, fast or slow. The slow mode provides the maximum power conservation during battery operation.

Wini Powerdown

This field allows you to set the amount of time the hard disk will continue to spin after the last disk activity. Setting the value to *"Always Off"* turns the hard disk off while setting this value to *"Always On"* causes the hard disk to remain on continuously *while power is applied to the computer. Use the space bar to increase the time and the BACKSPACE key to decrease the time in intervals of five seconds.*

Ext. Floppy

This field is used to identify what type of external floppy disk drive is attached to the computer: 5-1/4 inch 360K, 5-1/4 inch 1.2M, 3-1/2 inch 720K, or 3-1/2 inch 1.4M.

Video

The Video field allows you to choose between the built-in LCD or an external monitor attached to the video connector on the back panel. If the optional expansion chassis is attached to the computer, there are four additional selections available:

Color Card: 40x25 — This settings displays text at 40 characters per line, 25 lines per screen.

Color Card: 80x25 — This setting displays text at 80 characters per line, 25 lines per screen.

Mono Card: 80x25 — This setting selects a high-resolution monochrome display.

Enhanced Graphics — This setting selects an EGA or a high-resolution analog display.

Backlight

Use the Backlight field to set the time the backlight remains lit when there is no activity on the keyboard. Setting this value to *"Always Off"* turns the backlight off. Setting the value to *"Always On"* causes the backlight to remain on continuously. Turning the backlight off conserves power during battery operations *while power is applied to the computer. Use the space bar to increase the time and the BACKSPACE key to decrease the time in intervals of one minute.*

Boot

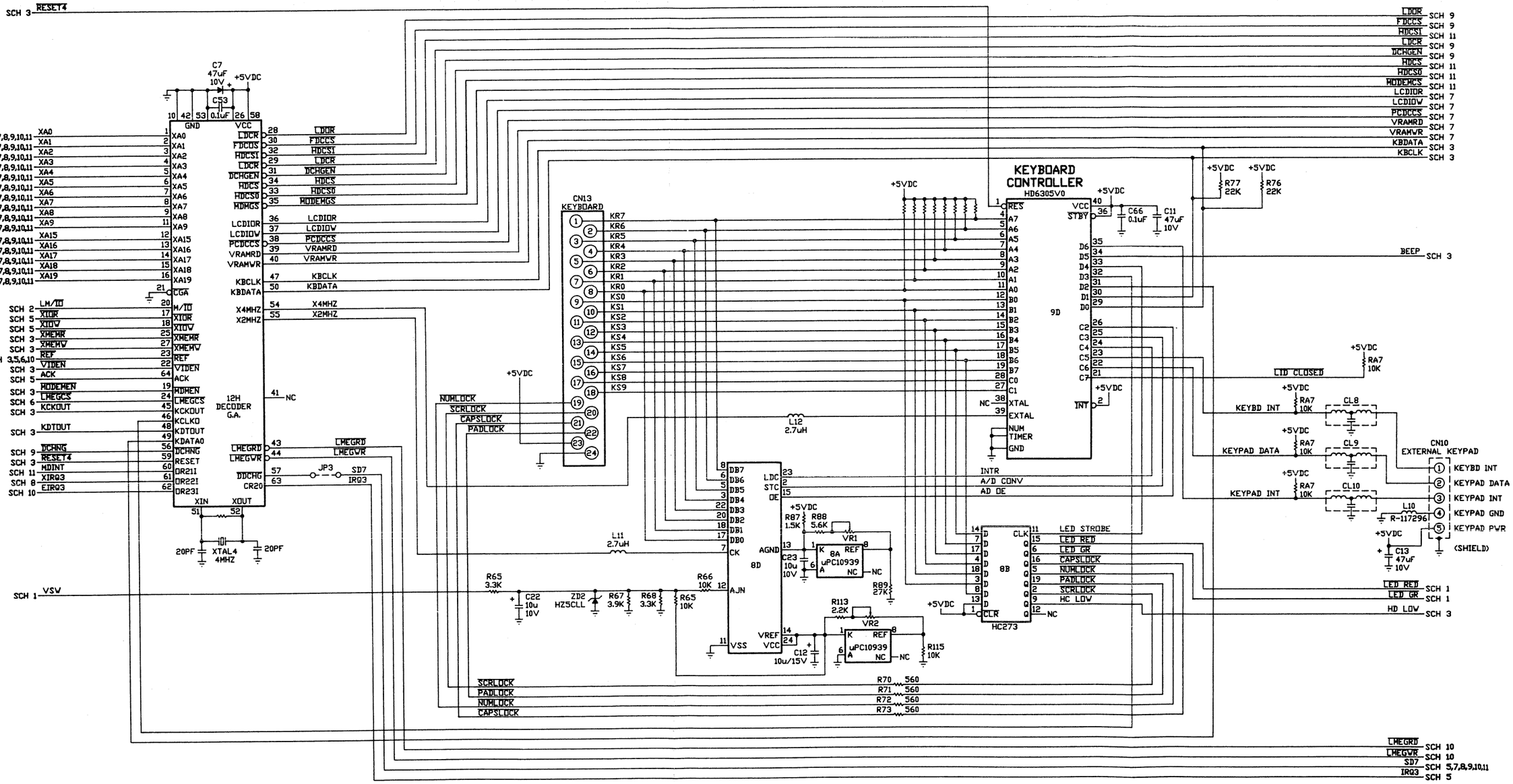
The Boot field allows you to select the drive your computer will attempt to boot from when it autoboots. You can select any of the following options:

Floppy Drive 0 — The computer will attempt to load the operating system from the floppy disk drive.

Hard Disk Drive 0 — The computer will attempt to load the operating system from the hard disk drive.

Floppy then Hard Disk — The computer will attempt to load the operating system from the floppy disk drive. If that drive is not ready, the computer will attempt to load the operating system from the hard disk drive.

Enter MFM-200 Monitor — This selection defeats autoboot. The computer will not attempt to load the operating system from either drive but will call up the Monitor program instead.



Schematic 4A

Major Integrated Circuits

The major ICs in the processor section of the computer are:

- The 80286 CPU
- An optional 80287 numeric coprocessor
- The 82C215 address/data buffer
- The 82C206 peripheral controller

The following sections describe the operation of these integrated circuits.

80286 CPU

✶ This computer uses the *Intel NMOS* 80286 microprocessor with a 16-bit data bus and a 24-bit address bus. The 80286 can also operate within an 8-bit architecture. It exercises all of the functions of a typical 8-bit microprocessor (8088) at an increased rate. Table 5-1 defines the pin functions and Figure 5-2 shows the pinout of the 80286 microprocessor.

✶ **Table 5-1. 80286 Microprocessor Pin Functions**

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1	$\overline{BHE}$	This output indicates transfer of data on bits D8 - D15. Byte-oriented devices residing on bits D8 - D15 use $\overline{BHE}$ to condition chip select functions.
2, 3	NC	These pins are not connected.
4, 5	$\overline{S1}$, $\overline{S0}$	CPU status lines that distinguish between read and write operations.
✶ 6	$\overline{PEACK}$	The 80286 asserts the $\overline{PEACK}$ signal to acknowledge $\overline{PEREQ}$.
7, 8	A23 - A22	CPU address bits 23 and 22.
9	VSS	Ground
10-28	A21 - A3	CPU address bits 3 through 21.

Table 5-1 (continued). 80286 Microporcessor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
29	RESET	This input causes a system reset to clear the internal logic of the 80286 (active-high). ✶
30	VCC	+5 VDC power supply.
31	CLK	System clock. This signal provides fundamental timing for the operation of the 80286. ✶
32-34	A2 - A0	CPU address bits 0 through 2.
35	VSS	Ground.
36-51	D0 -D15	CPU data bits 0 through 15.
52	CAP	A 0.047 µF capacitor must be connected between this pin and ground to filter the output of the internal bias generator.
53	$\overline{ERROR}$	Numeric processor extension error. Tied high in this computer.
54	$\overline{BUSY}$	Numeric processor extension busy. An active $\overline{BUSY}$ signal causes the 80286 to stop its program execution if the WAIT instruction or some ESC instructions are received. ✶
57	INTR	Interrupt request. This line conducts interrupt requests to the 80286, which cause it to suspend its current program execution and enter an interrupt service routine. ✶
59	NMI	Non-maskable interrupt.
60	VSS	Ground.
61	$\overline{PEREQ}$	Processor extension request. When $\overline{PEREQ}$ is high, the 80287 request the 80286 to allow it to assume program execution for a numeric operation. ✶

Table 5-1 (continued). 80286 Microporcessor Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
62	VCC	+5 VDC power supply.
63	$\overline{\text{READY}}$	Bus ready. When high, bus cycles are extended without limit. The bus cycle terminates once this line is forced low again.
64	HOLD	Hold. This active high input allows the bus controller to request control of the system bus.
65	HOLDA	Hold acknowledge. This output signal informs the bus controller that its request for control of the system bus has been granted.
66	COD/$\overline{\text{INTA}}$	Not connected.
67	M/$\overline{\text{IO}}$	Memory or input/output select. CPU status line that distinguishes between memory and input/ output operations.
68	$\overline{\text{LOCK}}$	Not connected.

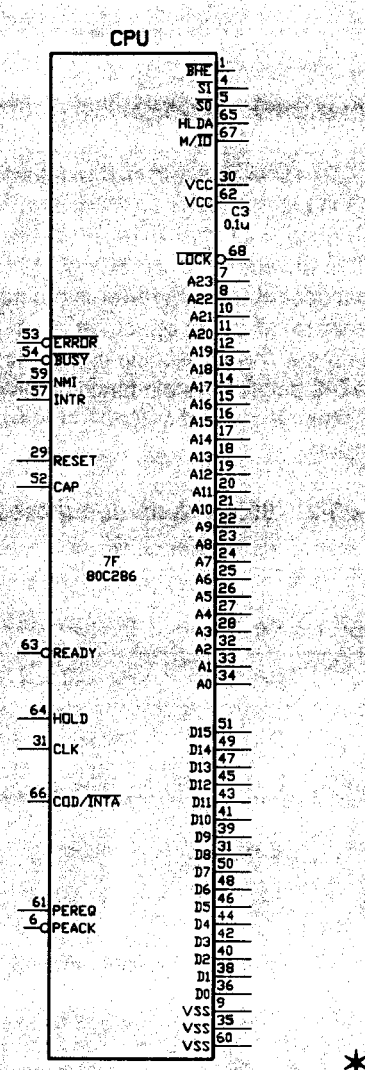


Figure 5-2. 80286 Microprocessor Pinout

Optional 80287 Numeric Processor Extension

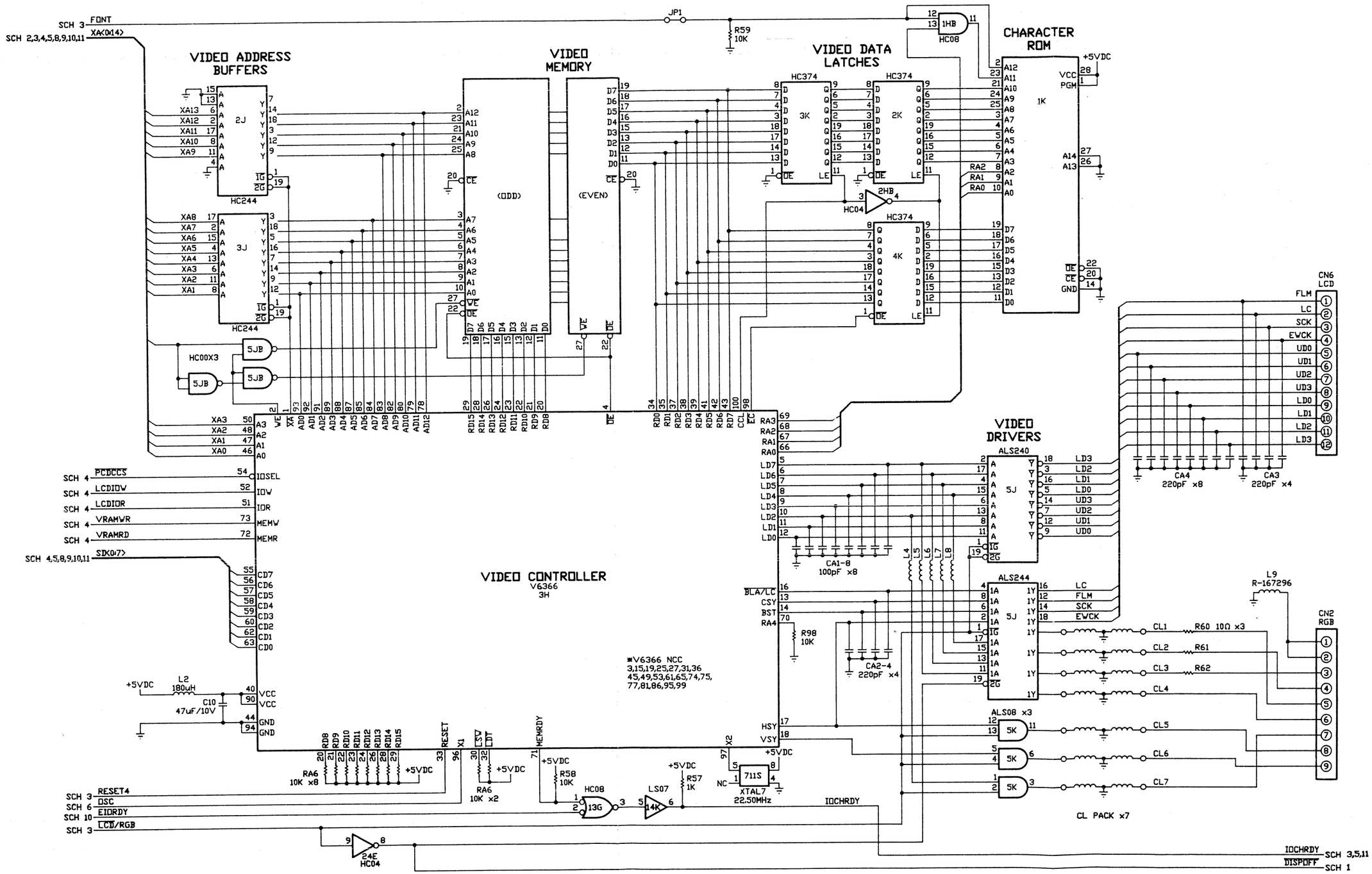
An 80287 numeric processor extension may be installed in the computer as an option. The instruction set for the 80287 contains over fifty additional instructions and its architecture allows it to perform complex mathematical operations with fewer instructions. The 80286 can perform all of the operations of the 80287 but requires many more machine cycles for each operation. Table 5-2 defines the pin functions and Figure 5-3 shows the pinout of the 80287 numeric processor extension.

Table 5-2. 80287 Numeric Processor Extension Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
1-4	NC	Not connected.
5-8	D12-D15	CPU data bits 12 through 15.
9	VCC	+5 VDC power supply.
10	VSS	Ground.
11, 12	D10-D11	CPU data bits 10 and 11.
13	NC	Not connected.
14-23	D0-D9	CPU data bits 0 through 9.
24	PEREQ	Processor extension request. This request indicates to the 80286 that the 80287 is ready to execute a numeric operation.
25	$\overline{\text{BUSY}}$	80287 busy. This signal indicates to the 80286 that the 80287 is currently executing a command.
26	$\overline{\text{ERROR}}$	This signal indicates that an unmasked error condition exists.
27	$\overline{\text{NPRD}}$	Numeric processor read. This signal enables transfer of data from the 80287.

Figure 5-2 (continued). 802 Numeric Processor Extension Pin Functions

PIN NUMBER	SIGNAL NAME	DESCRIPTION
28	$\overline{\text{NPWR}}$	Numeric processor write. This signal allows transfer of data to the 80287.
29	CMD0	Command line 0. This command line, with command line 1, $\overline{\text{NPS1}}$, and NPS2, allows the 80286 to direct operations to the numeric processor.
30	VSS	Ground.
31	CMD1	Command line 1. This command line, with command line 0, $\overline{\text{NPS1}}$, and NPS2, allows the 80286 to direct operations to the numeric processor.
32	CLK	This clock input provides the fundamental timing for internal 80287 operations.
33, 34	NPS2	Numeric processor select signals.
	$\overline{\text{NPS1}}$	If $\overline{\text{NPS1}}$ is low and NPS2 is high, the 80287 can perform floating point instructions.
35	RESET	80287 reset. This signal causes the 80287 to terminate its current program execution and enter a dormant state.
36	$\overline{\text{PEACK}}$	This signal acknowledges to the 80287 that its request signal (PEREQ) has been recognized. If there are no more numeric operations pending, the request signal will be withdrawn.
39	CKM	This signal is tied low in this computer.
40	NC	Not connected.



SWL-200-2/4 Portable Computer
Effective **June 1988**

Schematic 7A